University of Mumbai

Examination 2020 under Cluster 06

Examinations Commencing from 7th January 2021 to 20th January 2021

Program: **Electronics Engineering**

Curriculum Scheme: Rev 2019

Examination: SE Semester III

Course Code: ELC303 and Course Name: Digital Logic Circuits

Time: 2 hours Max. Marks: 80

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Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	Convert Decimal$(105)_{10}$ to Binary
Option A:	$(101001)_2$
Option B:	$(1101001)_2$
Option C:	$(1110101)_2$
Option D:	$(1001011)_2$
2.	Find 2's complement of $(11000100)_2$
Option A:	$(00111011)_2$
Option B:	$(11000101)_2$
Option C:	$(00111100)_2$
Option D:	$(00111011)_2$
3.	The logic expression AB +A'B' can be implemented by giving the inputs A and B to a two input
Option A:	NOR gate
Option B:	NAND gate
Option C:	X-OR gate
Option D:	X-NOR gate
4.	The logic expression f = B C+ $\bar{A}$B+ $\bar{A}$C is in
Option A:	SOP form
Option B:	POS form
Option C:	Standard SOP form
Option D:	Standard POS form
5.	The simplified form of the Boolean expression i (X + Y+ XY) (X + Z) is
Option A:	X + Y+ Z
Option B:	XY + YZ
Option C:	X + YZ
Option D:	XZ+Y
6.	A multiplexer with 3 select bits is a
Option A:	4:1 multiplexer
Option B:	8:1 multiplexer
Option C:	16:1 multiplexer

Option D:	32:1 multiplexer
7.	IC 7485 is a
Option A:	4 bit comparator IC
Option B:	4 bit adder IC
Option C:	4 bit subtractor IC
Option D:	decoder IC
8.	How many AND, OR and EX-OR gates are required for the configuration of full adder?
Option A:	1, 2, 2
Option B:	2, 1, 2
Option C:	3, 1, 2
Option D:	4, 0, 1
9.	Master Slave JK flipflop is used to avoid _____ in case of level triggered JK flipflop.
Option A:	Lock out condition
Option B:	Race around condition
Option C:	Forbidden condition
Option D:	Don't care condition
10.	For 3 bit asynchronous counter with negative edge triggered flipflops, cascaded input taken from Q and final output taken from Qbar, the counter will count_____
Option A:	Up
Option B:	UP-down
Option C:	Down
Option D:	Random
11.	6-bit Johnson counter will give module _____counter.
Option A:	6
Option B:	3
Option C:	24
Option D:	12
12.	1. When Two states are said to be equivalent in FSM?

Option A:	When they have same output for the given combination of inputs.
Option B:	When they have same next state and same output for the given combination of inputs.
Option C:	When they have same next state for the given combination of inputs.
Option D:	When they have same inputs.
13.	In case of _____output is delayed by one clock cycle.
Option A:	Decoder
Option B:	Multiplexer
Option C:	Moore Machine
Option D:	Mealy Machine
14.	In 74163 when the count is equal to 15 _____ output pin becomes one.
Option A:	RCO
Option B:	LD
Option C:	CLR
Option D:	ENP
15.	In PAL 10 X 4 What X indicates?
Option A:	An Array of AND-Ex-OR and Flipflop
Option B:	An Array of AND-OR and Flipflop
Option C:	An Array of OR-AND and Flipflop
Option D:	An Array of Ex-OR-AND and Flipflop
16.	TTL logic family gives inbuilt Noise margin of _____
Option A:	0.2V

Option B:	0.1V
Option C:	0.5V
Option D:	0.4V
17.	For CMOS-TTL interfacing _____ is used to solve current related interfacing problems.
Option A:	Buffer
Option B:	Amplifier
Option C:	Multiplexer
Option D:	Flipflop
18.	_____ is a net data type used in Verilog.
Option A:	reg
Option B:	integer
Option C:	real
Option D:	wire
19.	12'o1345 indicates _____in Verilog
Option A:	12 bit octal number
Option B:	16 bit octal number
Option C:	12 bit hexadecimal number
Option D:	16 bit hexadecimal number
20.	In procedural assignment type _____ data type is used.
Option A:	reg
Option B:	wire
Option C:	wor
Option D:	tri

Q2.A	**Solve any Two 5 marks each**
i.	NAND is called as universal Gate .Justify your answer.
ii.	Explain TTL -CMOS interfacing
iii.	Minimize the following expression using k-map and Implement Using basic gates. F(A,B,C,D)=∑m(1,2,7,9,10,11,14,15)+d(4,5)
Q2.B	**Solve any One** **10 marks each**
i.	Design synchronous decade counter using T flipflops
ii.	Minimize the given state table and write reduced state table using implication chart method.

Present State	Next State x=0	Next State x=1	Output
A	B	C	1
B	D	F	1
C	F	E	0
D	B	G	1
E	F	G	0
F	E	D	0
G	F	G	0

Q3.A	**Solve any Two 5 marks each**
i.	Write a note on CPLD
ii.	Write Verilog code for 4:1 multiplexer and 4bit binary counter
iii.	Convert D Flip-Flop into T Flip-Flop
Q3.B	**Solve any One** **10 marks each**
i.	Design MOD-78 counter using IC7490.
ii.	Design Full Subtractor using IC 74138(3:8 Decoder).