University of Mumbai

Examinations Commencing from 22nd November 2021 to 5th January 2022

Program: Electronics and Computer Science

Curriculum Scheme: Rev2019

Examination: SE Semester III

Course Code: ECC303 and Course Name: Digital Electronics

Time: 2hour 30 minutes Max. Marks: 80

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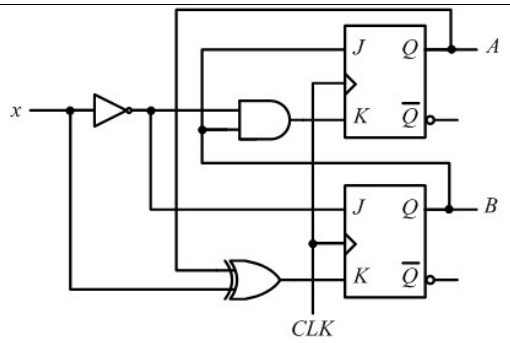
Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	What is the reflected binary code of $(100101)_{2.}$
Option A:	111000
Option B:	101010
Option C:	101111
Option D:	110111
2.	How many two-input AND and OR gates are required to realize Y = AB+CD+E?
Option A:	2,2
Option B:	2,3
Option C:	3,2
Option D:	3,3
3.	If a half adder has A and B as the inputs, then the product is given by
Option A:	A EX-NOR B
Option B:	A OR B
Option C:	A AND B
Option D:	A XOR B
4.	What are the number of select lines required for a 16:1 multiplexer?
Option A:	1
Option B:	2
Option C:	3
Option D:	4
5.	A demultiplexer converts _____inputs to multiple outputs.
Option A:	2
Option B:	1
Option C:	2n
Option D:	2^n
6.	A BCD counter can be implemented with how many number of flip flops?
Option A:	10
Option B:	5
Option C:	4
Option D:	8

7.	In a sequential circuit designed as a mealy machine, the output depends on
Option A:	present state
Option B:	past state
Option C:	Present state and input
Option D:	external inputs
8.	The internal structure of MSI counter IC 7493 consist of
Option A:	Mod 2 and Mod 6 counter
Option B:	Mod 2 and Mod 8 counter
Option C:	Mod 5 and Mod 8 counter
Option D:	Mod 2 and Mod 5 counter
9.	What does CPLD stand for
Option A:	Complex Programmable Logic Device
Option B:	Combinational Programmable Logic Device
Option C:	Combined Preset Logic Device
Option D:	Complex Preset Logic Device
10.	In verilog HDL the operator <= is used for
Option A:	Blocking assignment
Option B:	Non-Blocking assignment
Option C:	Single line comment
Option D:	Logical left shift

Q2. **(20 Marks)**	
A	**Solve any Two (5 marks each)**
i.	Design and implement a half subtractor using gates.
ii.	Draw the table for Boolean Subtraction
iii.	Compare combinational and sequential circuits.
B	**Solve any One (10 marks each)**
i.	Design a Mod-12 asynchronous counter using J-K Flip–Flops.
ii.	Write a program using Verilog HDL to implement a 8:1 multiplexer.

Q3. **(20 Marks)**	
A	**Solve any Two out of Three (10 marks each)**
i.	Design and implement half subtractor circuit using a 3:8 decoder IC 74138.
ii.	Analyze the given state machine and draw the state diagram.

	
iii	Design a Ring Counter using D Flip Flops.

Q4. **(20 Marks)**	
A	**Solve any Four out of Six (5 marks each)**
i.	Explain with neat diagrams working of IC7483
ii.	State the differences between mealy and moore machine.
iii.	Write a short note on Complex Programmable Logic Devices.
iv	Explain with suitable diagrams working of IC74163.
v	Write a program using Verilog HDL for implementing a 8:1 Multiplexer
vi	Explain in brief about the interfacing of CMOS to TTL ICs.