**Program: BE Electronics and Telecommunication Engineering**

**Curriculum Scheme: Revised 2012**

**Examination: Second Year Semester III**

**Course Code: ETS303** **Course Name: Digital Electronics**

**Time: 1 hour** **Max. Marks: 50**

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**Note: All the questions are compulsory and carry equal marks.**

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| Q.1 | Which of the following is the hexadecimal equivalent of $(2598.675)_{10}$ |
| Option A: | $(B26.BDDD)_{16}$ |
| Option B: | $(A26.ACCC)_{16}$ |
| Option C: | $(B25.BDDC)_{16}$ |
| Option D: | $(A26.ADDC)_{16}$ |
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| Q.2 | What is the binary equivalent of $(105.15)_{10}$ |
| Option A: | (1100001.001001)2 |
| Option B: | (1101001.001001)2 |
| Option C: | (1110101.001011)2 |
| Option D: | (1001101.001011)2 |
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| Q.3 | The Boolean Expression PQ'R (QS + RST) + PR' simplifies to |
| Option A: | P + Q'RST |
| Option B: | P (R' +QST) |
| Option C: | PR + QST |
| Option D: | P (R'+Q'ST) |
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| Q.4 | Which of the following statements is not correct? |
| Option A: | AB + A'C + BC = AB + A'C |
| Option B: | A + AB = A |
| Option C: | (A + B) (A' + C) (B + C) = (A + B) (A' + C) |
| Option D: | AB + A'C = (A + C') (A' + B') |
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| Q.5 | Which of the following represents the Sum of Products expression for the function $f(W, X, Y, Z) = \sum(0,1,2,8,11) + d(3,9,15)$ |
| Option A: | W'X' +X'Y' + X'Z |
| Option B: | W'X' +WYZ |
| Option C: | W'X' +X'Y' + Z |
| Option D: | W'X' +WYZ + X'Z |

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| Q.6 | Which of the following is not a property of CMOS logic gates? |
| Option A: | High switching speed |
| Option B: | Low static power consumption |
| Option C: | High packing density |
| Option D: | High noise margin |
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| Q.7 | If I want to implement a logic circuit using a single logic gate that takes two inputs A and B and gives an output '1' if A is equal to B, else gives an output '0', which of the following logic gate should be used? |
| Option A: | AND gate |
| Option B: | OR gate |
| Option C: | XOR gate |
| Option D: | XNOR gate |
| | |
| Q.8 | Which digital circuit acts as switch.? |
| Option A: | Comparator |
| Option B: | Counter |
| Option C: | De-Multiplexer |
| Option D: | Multiplexer |
| | |
| Q.9 | What is 2's Complement of Binary number 0000 1000 ? |
| Option A: | 1110 1000 |
| Option B: | 1111 1000 |
| Option C: | 1010 1100 |
| Option D: | 1110 0011 |
| | |
| Q.10 | Assume that a particular IC has a supply voltage (Vcc) equal to +5 V and ICCH = 10 mA and ICCL = 23 mA. What is the power dissipation for the chip? |
| Option A: | 50 mW |
| Option B: | 82.5 mW |
| Option C: | 115 mW |
| Option D: | 155 mW |
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| Q.11 | A circuit that converts n inputs to 2^n outputs is called |
| Option A: | Encoder |
| Option B: | Decoder |
| Option C: | Multiplexer |
| Option D: | carry look ahead |
| | |
| Q.12 | Output of comparator when A = 1010 and B = 1011 is _____. |
| Option A: | A > B = 1, A < B = 0, A = B = 1. |
| Option B: | A > B = 0, A < B = 1, A = B = 0. |
| Option C: | A > B = 1, A < B = 0, A = B = 0. |
| Option D: | A > B = 0, A < B = 1, A = B = 1. |
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| Q.13 | Two 4-bit binary numbers A = 1011 and B = 1111 are applied to a 4-bit parallel adder. The carry input is 1. What are the values for the sum and carry output? |
| Option A: | S4 S3 S2 S1 = 0111, Cout = 0. |
| Option B: | S4 S3 S2 S1 = 1111, Cout = 1. |
| Option C: | S4 S3 S2 S1 = 1011, Cout = 1. |
| Option D: | S4 S3 S2 S1 = 1100, Cout = 1. |
| | |
| Q.14 | An SR latch is created using only two NOR gates with S and R inputs feeding one NOR gate each. If both S and R inputs are set to one, the outputs will be |
| Option A: | Q and Q' complementary to each other |
| Option B: | Q and Q' both 1 |
| Option C: | No change in circuit output |
| Option D: | Q and Q' both 0 |
| | |
| Q.15 | Which of the following statements is NOT correct? |
| Option A: | Race around condition occurs in a JK latch when both the inputs are one. |
| Option B: | A flip flop is used to store one bit information. |
| Option C: | A transparent latch is Dtype flipflop with enable (level triggered) in place of a clock. |
| Option D: | Masterslave configuration is used in flipflop to store two bits information. |
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| Q.16 | The complex programmable logic device contains several PLD blocks and _____ |
| Option A: | A language compiler |
| Option B: | AND/OR arrays |
| Option C: | Global interconnection matrix |
| Option D: | Field-programmable switches |
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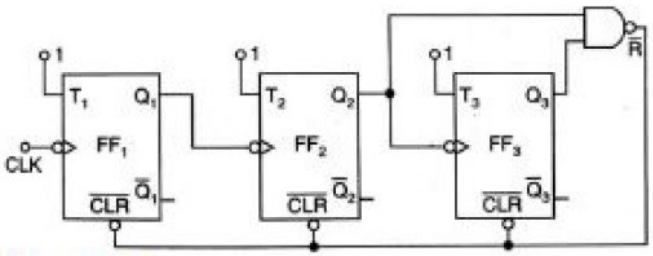
| Q.17 | A sequential access memory is one in which _____ |
| Option A: | A particular memory location is accessed rapidly |
| Option B: | A particular memory location is accessed sequentially |
| Option C: | A particular memory location is accessed serially |
| Option D: | A particular memory location is accessed parallel |
| | |
| Q.18 | Non-volatile memory refers to _____ |
| Option A: | The memory whose loosed data is retained again when power to the memory circuit is removed/applied |
| Option B: | The memory which looses data when power to the memory circuit is removed |
| Option C: | The memory which looses data when power to the memory circuit is applied |
| Option D: | The memory whose loosed data is achieved again when power to the memory circuit is applied |
| | |
| Q.19 | The following circuit is a   a. Synchronous Mod 7 counter<br>b. Asynchronous Mod 7 counter<br>c. Synchronous Mod 6 counter<br>d. Asynchronous Mod 6 counter |
| Option A: | a |
| Option B: | b |
| Option C: | c |
| Option D: | d |

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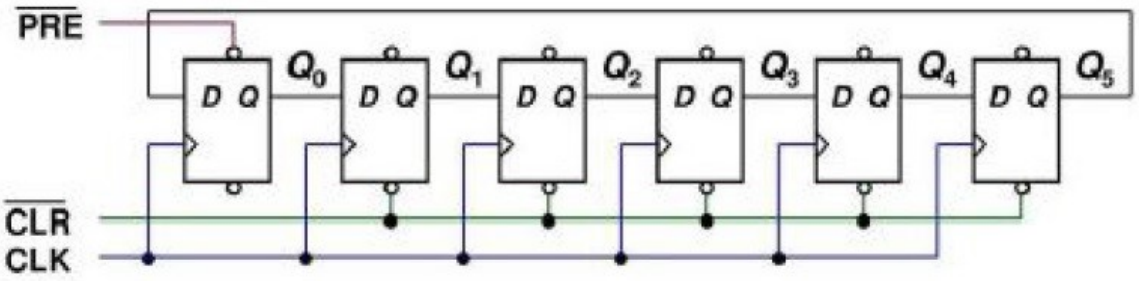
| Q.20 | The following circuit is a<br>  <br><br>a. Mod-6 Ring Counter<br>b. Mod-6 Johnson Counter<br>c. Mod-12 Ring Counter<br>d. Mod-12 Johnson Counter |
| Option A: | a |
| Option B: | b |
| Option C: | c |
| Option D: | d |
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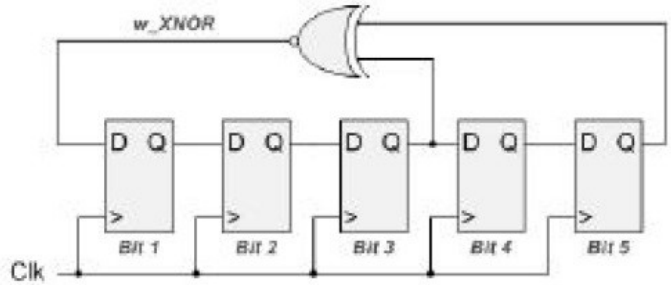
| Q.21 | If the initial values of the flip-flops are 10110 from right to left, then after 3 clock cycles their values will be<br>  <br><br>a. 10110<br>b. 00101<br>c. 10010<br>d. 01011 |
| Option A: | a |
| Option B: | b |
| Option C: | c |
| Option D: | d |
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| Q.22 | How many flip-flops are required to count $32767_{10}$ using a binary ripple counter?<br>a. 15<br>b. 16<br>c. 17<br>d. 20 |
| Option A: | a |
| Option B: | b |
| Option C: | c |
| Option D: | d |
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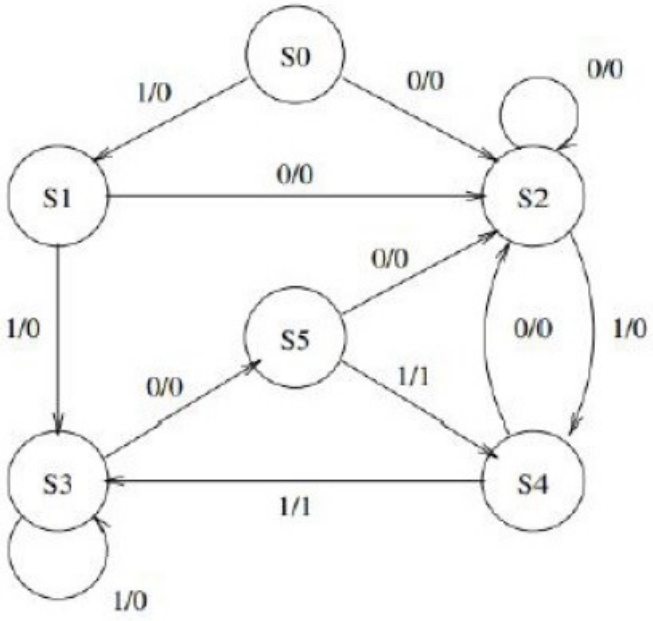
| Q.23 | Let X is the input sequence whereas Z is the output sequence for the state machine shown below. Which of the following options correctly describes the output Z sequence for input sequence X given below (Assume initial state S0)<br>X = 0 0 1 1 0 1 1 0 1 0 1 1 0 1 0<br>  <br><br>a. Z = 0 0 0 1 0 1 1 0 1 0 0 1 0 1 0<br>b. Z = 0 0 0 1 0 0 1 0 0 0 0 1 0 0 0<br>c. Z = 0 0 0 0 0 1 0 0 1 0 0 0 0 1 0<br>d. Z = 0 0 1 0 1 1 0 1 0 0 1 0 1 0 0 |
| Option A: | a |
| Option B: | b |
| Option C: | c |
| Option D: | d |
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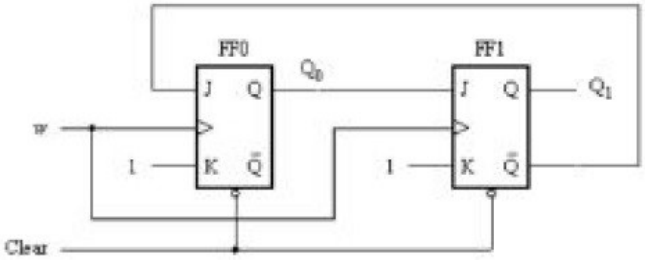
| Q.24 | What function is implemented by the circuit shown below? Assume the signal **w** is driven by a square wave signal.<br>  <br><br>a. Modulo -3 counter<br>b. Modulo-4 counter<br>c. Modulo-5 counter<br>d. Modulo-6 counter |
| Option A: | a |
| Option B: | b |
| Option C: | c |
| Option D: | d |
| Q.25 | If I want to divide 10110100 by 4 using shift register, I have to perform<br>a. 1-bit left shift<br>b. 1-bit right shift<br>c. 2-bit left shift<br>d. 2-bit right shift |
| Option A: | a |
| Option B: | b |
| Option C: | c |
| Option D: | d |