02/06/17

Scm 6 Extc

Q.P. Code :11990

[Time: 3 Hours] [ Marks:80]

Please check whether you have got the right question paper.

N.B:
1. Questions number 1 is compulsory.
2. Solve any three questions from the remaining
3. Illustrate your answer with neat sketches

Q.1 A Write characteristics of D2 MAC. 4
B How is charge image created in image orthicon? 4
C Briefly explain NTSC coder? 4
D What is the use of front porch and back porch in the composite video signal? 4
E What is the need of MUSE system? 4

Q.2 A Why are color difference signals used in colors transmission? Why (G-Y) is not transmitted in color TV. Elaborate? 10
B Explain working of vidicon camera tube? 10

Q.3 A A draw and explain working principle of LCD display. Compare and contrast LCD and LED televisions? 10
B Explain the concept of frequency interleaving. What is the need of interlaced scanning? 10

Q.4 A Discuss composite video signal with respect to blanking level, pedestal height, active period and black and white level? 10
B What is the need of multiplexed analog component? Explain MAC signal? 10

Q.5 A In relation to digital TV discuss? 10
1) Pixel array
2) Viewing angle and distance
3) Digitization
4) Frame rate and refresh rate

Q.5 B What is need of chroma sub sampling? Explain types of chroma sub sampling? 10

Q.6 Write short note on
1 Direct to home television 7
2 Plasma television 7
3 Compatibility and reverse compatibility? 6

Sem-VI
EXTC (CBGS)

22/05/17

T3126 / T0891 DISTRICT TIME SIGNAL PROCESSING

DTSP

Q.P.Code:16204

**(3 hours)** **[Total Marks: 80]**

N.B: 1) Question number **1 is compulsory**
2) Solve any **three** questions out of the remaining **five** questions
3) In all four questions to be attempted.
4) **Figures** to the **right** indicate full marks

Q.1 (a) Derive relationship between DFT and DTFT. (05)

(b) Compare: Impulse invariant technique and bilinear transformation technique. (05)

(c) Define phase delay and group Delay. (05)

(d) Explain interpolation process with frequency spectrum. (05)

Q2) (a) Develop **Composite radix DITFFT** flow graph for **N= 6 =2 ×3** (10)

(b) Analog filter Transfer function is $H(s) = \frac{4}{(S+1)(S^2+4S+5)}$ obtain equivalent digital filter transfer function H(Z) using impulse invariant technique by taking T=0.5 sec (10)

Q.3 (a) State two important properties of DFT which are used to derive FFT. How Computational Complexity of DITFFT algorithm is determined from flow graph. Derive necessary formulas. (10)

(b) $y(n) = 2x(n) + \frac{4}{5}x(n-1) + \frac{3}{2}x(n-2) + \frac{2}{3}x(n-3)$ (10)

Determine lattice realization.

Q.4 (a) Using frequency sampling method, design FIR band pass filter for following specifications

Sampling frequency =8000Hz

Cut Off frequency =$f_{c_2}$=3000Hz

Cut Off frequency =$f_{c_1}$=1000Hz

Determine filter coefficients for N=7 (10)

(b) Write short note on: Dual tone multi frequency detection (06)

(c) What is multi rate DSP? State its applications. (04)

Q(5) (a) Design a Butterworth digital IIR filter using BLT by taking T = 0.1sec to satisfy following specifications (10)

$0.6 \leq |H(e^{jw})| \leq 1.0$ $\quad 0 \leq w \leq 0.35\pi$

$|H(e^{jw})| \leq 0.1$ $\quad 0.7\pi \leq w \leq \pi$

Turn Over

(b) x(n) ={ 2,3.4,5} and y(n)={5,2,3,4) (10)

(i) Find circular convolution using time domain method

(ii) Find circular convolution using frequency domain method

(iii) Compute linear convolution. Comment on your results.

Q6) (a) The transfer function for discrete time causal system is given by (10)

$$H(z) = \frac{1-z^{-1}}{1-0.2z^{-1}-0.15z^{-1}}$$

(i)Find difference equation

(ii) Draw Direct Form-I and Direct form-II realization structure

(iii)Draw cascade and parallel realization

(b) Explain the effects of coefficients quantization in FIR filters (05)

(c) State Parserval's theorem. Verify it for x (n) = {1, 2, 3, 4} (05)

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VI e EXTC CBGS 26/05/17



**Q. P. Code : 13294**

**( 3 Hours )** **( Total Marks: 80**

**N.B. :**

**(a) Question No.1 is compulsory.**
**(b) Total 4 questions need to be solved.**
**(c) Attempt any three questions from remaining five questions.**
**(d) Assume suitable data wherever necessary, justify the same.**

| | | |
|---|---|---|
| 1.a | Which is better, ADSL or cable? Justify your answer. | [5] |
| 1.b | Explain the persistent strategies of CSMA. | [5] |
| 1.c | Explain the fields that are related to Fragmentation and Reassembly of an IPv4 datagram. | [5] |
| 1.d | Discuss Quality of Service (QoS) in terms of Flow characteristics. | [5] |
| 2.a | Explain the concept of sending an E-mail using an appropriate Application layer protocol. | [10] |
| 2.b | Explain with diagram the connection establishment and connection termination in TCP using Three- Way Handshaking. | [10] |
| 3.a | Explain how BGP achieves Inter-Autonomous System Routing. | [10] |
| 3.b | With an example explain the concept of building a routing table in Link state Routing. | [10] |
| 4.a | What is Peer to Peer(P2P) File sharing. Differentiate between the centalized and decentralized P2P. | [10] |
| 4.b | Explian various networking devices. | [10] |
| 5.a | Draw the header of IPv6. Explain each field. | [10] |
| 5.b | Explain in detail 802.11 Wireless LAN. | [10] |
| 6 | Write a short notes on : (a) Flow control using TCP (b) Wi Max (c) MPLS (d) DNS | [20] |

VI EXTC CBGS 16/5/17

DC

Q.P.Code: 013273

(3 Hours) [Total Marks: 80]

N.B.
1] Question no.1 is **compulsory**
2] Attempt any **three** questions out of remaining **five** questions
3] Assumptions made should be **clearly** stated
4] Illustrate answers with **sketches** wherever **required**

Q.1 Attempt any **four**

a Prove that entropy of extremely unlikely messages is zero. 5

b Compare offset QPSK and non-offset QPSK. 5

c State two criteria which a spread-spectrum communication system must satisfy. Justify that the spread-spectrum signals are transparent to the interfering signals, and vice-versa. 5

d Explain the Coherent and non-coherent digital modulation techniques. 5

e Prove that syndrome depends on error patterns and not on transmitted code word. 5

Q.2

a Consider the five source symbols of a discrete memoryless source and their respective probabilities as below. 10

| $S_i$ | $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ |
|---|---|---|---|---|---|
| P(si) | 0.4 | 0.2 | 0.2 | 0.1 | 0.1 |

i) Create a Huffman Tree for Huffman source coding technique to find the codeword and length of codewords for each source symbol.
ii) Determine the average codeword length of the specified discrete memoryless source.
iii) Comment on the results obtained

b Describe in convolution code, Time domain approach, and Transform-domain approach to determine encoder output. 10

Q.3

a Justify that the probability of error in matched filter does not depend on the shape of input signal. Derive the relevant expression. 10

b Explain the working of M-ary PSK Transmitter and receiver and plot spread spectrum and calculate the bandwidth.. 10

Q.4

a Describe coherent detection method of binary FSK signals. Also draw power spectra for BFSK modulated signal. 10

b In a digital communication system, the bit rate of a bipolar NRZ data sequence is 1 Mbps and carrier frequency of transmission is 100MHz. Determine the symbol rate of transmission and the bandwidth requirement of the communications channel for 10
i) 8-ary PSK system
ii) 16-ary PSK system.

**TURN OVER**

Q.5

a Design a syndrome calculator for a (7, 4) Hamming code, generated by the generator polynomial $g(x)=1+X^2+X^3$ , if the transmitted code word C=(0111001) and received word r = (0110001). 10

b A (7, 4) cyclic code is described by a generator polynomial 10

$$g(x) = x^3 + x + 1$$

i) Find out the generator matrix

ii) Parity checks matrix.

iii) Draw the syndromecalculator and explain how received message is corrected?

Q.6 **Attempt the following (any two).**

a Write short note on Intersymbol interference (ISI) and Eye diagram. 10

b Explain with the help of block diagrams and waveforms, the following techniques of spread spectrum communication. (a) Direct sequence (b) Frequency hopping. 10

c What are different decoding methods of convolutional codes? Explain any one in detail. 10

08/06/17

Sem VI EXTC (CBGS)

Q.P. Code :13893

[Time: Three Hours] [ Marks:80]

Please check whether you have got the right question paper.

N.B:
1. Question.No.1 is compulsory.
2. Attempt any 3 questions from the remaining 5 questions.
3. Draw neat diagrams wherever necessary.

| | | | |
|---|---|---|---|
| Q.1 | a) | What is operating system? Discuss the role of an OS as a resource manager. | 5 |
| | b) | Differentiate between deadlock avoidance and deadlock prevention. | 5 |
| | c) | What are the advantages of Linux and Unix over windows? | 5 |
| | d) | Explain the performance of demand paging. | 5 |
| Q.2 | a) | Explain clearly, how Unix performs file management using I-nodes. | 10 |
| | b) | What is process? Explain the life cycle of a process using process state transition diagram. | 10 |
| Q.3 | a) | Explain clearly, paging and segmentation based memory management techniques. | 10 |
| | b) | Explain the working of Buddy algorithm in Linux memory management. | 10 |
| Q.4 | a) | What is semaphore? Give an implementation of bounded buffer producer consumer problem using semaphore. | 10 |
| | b) | Explain the different methods of organizing directories in an operating system. | 10 |
| Q.5 | a) | What is kernel of an operating system? What are the different types of kernels? | 10 |
| | b) | Explain the working of EDF and RMA real time scheduling algorithms. | 10 |
| Q.6 | | Write a details note on following | |
| | a) | Disks Arm Scheduling Algorithms. | 10 |
| | b) | Logical and physical address space. | 10 |

EXTC

14/06/17

T3126 / T0895 VLSI DESIGN

Sem-VI

**Q.P.Code:16055**

Q3. A. Design the circuit and draw layout for the function $Y = \overline{(D + E + F)(B + C + A)}$ using CMOS logic. Also find equivalent CMOS inverter circuit for simultaneous switching of all inputs assuming that $(W/L)_P$=30 for all PMOS transistors and $(W/L)_N$=10 for all NMOS transistors. **10 Marks**

B. What are the problems of Domino logic? Also suggest remedy for these problems. **10 Marks**

Q4. A. With neat diagrams explain the read and write operation of 3T DRAM cell. **10 Marks**

B. Explain in detail design strategy of 6T SRAM Cell. Also draw the layout for 6T SRAM cell. **06 Marks**

C. Draw MOSFET based Master Slave JK Flip Flop **04 Marks**

Q5. A. Construct the complementary static CMOS full adder. Now propose another full adder which will take less number of transistors as compared to complementary static CMOS full adder. **10 Marks**

B. Draw and explain 4 X 4 multiplier array. **06 Marks**

C. Justify that even if LEVEL 1 MOSFET model already exists there is necessity of LEVEL 2 MOSFET Model. **04 Marks**

Q6. A. With suitable diagrams explain clock stabilization in VLSI Chip. **05 Marks**

B. What is the need of input and output ports in CMOS circuits? Explain with neat schematic bidirectional IO port. **05 Marks**

C. Explain different components of leakage power in CMOS **05 Marks**

D. Explain DIBL and velocity saturation in short channel device. **05 Marks**

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**Q.P.Code:16055**

**Time: 3 Hours** **Marks: 80**

**Please check whether you have got the right question paper.**

N.B. : 1. Question No. ONE is compulsory
2. Solve any THREE out of remaining questions
3. Assume suitable data if required

Q1. Solve the following **20 Marks**

A. Show the current drawn by CMOS inverter on VTC and justify that CMOS inverter draws maximum current during switching.

B. Compare all types of MOSFET based inverters. Clearly draw their circuits and also mention their advantages and limitation/drawbacks.

C. Two lines on an interconnect level are separated a spacing of S=0.60 μm. Each individual line has w=0.30 μm, $T_{ox}$=1.0 μm and t=1 μm. Calculate the coupling capacitance per unit length $C_C$. Also find the coupling capacitance if the interaction length is 25 μm.

D. In short, explain what is pass transistor logic? With suitable example explain when you will prefer pass transistor logic and when transmission gate.

Q2. A. Calculate τfall using average current method for CMOS inverter with following parameters: **05 Marks**

Power supply voltage $V_{DD}$=3.2 V
Output load capacitance = 0.1 pF
$\mu_n C_{ox}$=20 μA/V2
$(W/L)_n$=20
$V_{T,n}$=1.0 V

B. For the function $Z = \overline{(A+B)(E+F)(H+I)}$ **05 Marks**

(i) Domino CMOS circuit

(ii) Draw an equivalent circuit for domino circuit by using equivalent transistor sizes with W/L=30/2 (both for NMOS and PMOS)

C. Design CMOS inverter such that the switching threshold is $V_{th}$ = 1.2 V, with the following device parameters:

NMOS: $V_{T0,n}$= 0.6 V $\mu_n C_{ox}$=60 μA/V$^2$
PMOS: $V_{T0,p}$= −0.8 V $\mu_p C_{ox}$=20 μA/V$^2$
Assume $V_{DD}$= 2.4 V and λ=0 **10 Marks**