University of Mumbai

Examination 2021 under cluster __(Lead College: _____)

Examinations Commencing from 15th June 2021 to 24th June 2021

Program: **BE Electronics & Telecommunication Engineering**

Curriculum Scheme: Rev 2019 'C' Scheme

Examination: SE Semester III

Course Code: **ECC301** and Course Name: **Engineering Mathematics III**

Time: 2 hour Max. Marks: 80

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Note: All Questions are compulsory.
Q1 carrying 40 marks. Q2 and Q3 are carrying 20 equal marks

Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	Find Laplace transform of $e^{-1(t}$
Option A:	$\frac{1}{s-10}$
Option B:	$\frac{1}{s+1(t}$
Option C:	$\frac{10}{s+10t}$
Option D:	$\frac{1}{s+10}$
2.	If $L[f(t)] = \frac{4s}{s^2-9}$, find $L[f(2t)]$
Option A:	$\frac{s}{s^2-36}$
Option B:	$\frac{4s}{s^2-36}$
Option C:	$\frac{4s}{s^2-9}$
Option D:	$\frac{4s}{s^2-18}$
3.	Find $L\left\|\frac{sint}{t}\right\|$
Option A:	$cot^{-1}(s)$
Option B:	$tan^{-1}(s)$
Option C:	$cot^{-1}\left(\frac{s}{a}\right)$
Option D:	Does not exists
4.	Find $L\left\|\int_0^t cos2udu\right\|$
Option A:	$\frac{s}{s^2+4}$

Option B:	$\frac{s}{s^2+1}$
Option C:	$\frac{1}{s^2+4}$
Option D:	$\frac{1}{s^2+1}$
5.	$L^{-1}\left\|\frac{4s-3}{s^2+9}\right\| = ?$
Option A:	$4cos3t - sin3t$
Option B:	$4cos3t + sin3t$
Option C:	$4cos3t - 3sin3t$
Option D:	$4sin3t - cos3t$
6.	Find $L^{-1}\left\|\frac{s+2}{s^2+4s+13}\right\|$
Option A:	$e^{2t}cos3t$
Option B:	$e^{-2t}cos3t$
Option C:	$e^{2t}sin3t$
Option D:	$e^{-2t}sin3t$
7.	In Fourier series of $f(x) = x + x^3$ in $(-\pi, \pi)$. The coefficient of $cos2x$ is
Option A:	-1
Option B:	$\frac{-1}{2}$
Option C:	1
Option D:	0
8.	$f(x) = x^2 + sinx$ is
Option A:	Even as well as odd function
Option B:	neither even nor odd function
Option C:	odd function
Option D:	Even function
9.	In the half range sine Series of $f(x) = x - x^2$ in (0 , 1) coefficient b_2 is
Option A:	0
Option B:	$\frac{1}{\pi^2}$
Option C:	$\frac{8}{\pi^3}$
Option D:	$\frac{4}{\pi^3}$
10.	A function f(t) is periodic with period 2π if
Option A:	$f(t + 2\pi) = 0$
Option B:	$f(t + 2\pi) = 2\pi$

Option C:	$f(t+2\pi) = f(2\pi)$
Option D:	$f(t+2\pi) = f(t)$
11.	Find the corresponding analytic function for harmonic function v = $3x^2y + 6xy - y^3$ is
Option A:	$z^3 - z^2 + c$
Option B:	$z^2 + 3z^3 + c$
Option C:	$z^3 + 3z^2 + c$
Option D:	$z^3 - 3z^2 + c$
12.	Which of the following statement is true
Option A:	A bilinear transformation is a combination of basic transformations translation, rotation and inversion
Option B:	A bilinear transformation is known as Mobius Transformation
Option C:	Every Bilinear transformation is conformal
Option D:	All options are TRUE
13.	If u and v are the harmonic functions then which of the following function is not harmonic function
Option A:	uv
Option B:	$u+v$
Option C:	$\frac{u}{v}$
Option D:	$u-v$
14.	Find the eigen values of matrix A, Where $A = \begin{vmatrix} 7 & 4 & -1 \\ 4 & 7 & -1 \\ -4 & -4 & 4 \end{vmatrix}$
Option A:	$\lambda = 3, 3, 12$
Option B:	$\lambda = 12, -3, -3$
Option C:	$\lambda = 7, 7, 4$
Option D:	$\lambda = -12, 3, 3$
15.	If $A = \begin{vmatrix} 1 & 2 \\ 2 & -1 \end{vmatrix}$ find A^4.
Option A:	$5I$
Option B:	$25I$
Option C:	$125I$
Option D:	$625I$

16.	If A = $\begin{vmatrix} 2 & 0 & 0 \\ 3 & -1 & 0 \\ -4 & 5 & 0 \end{vmatrix}$ Find Eigen Values of $A^2 + 2A + I$
Option A:	9,0,0
Option B:	9,0,1
Option C:	3,0,0
Option D:	9,4,1
17.	If the matrix A has eigen value -1,-1,2 then algebraic multiplicity of A for $\lambda = -1$ is
Option A:	-1
Option B:	0
Option C:	1
Option D:	2
18.	The divergence and curl of $\bar{a} = 3i - j + 2k$ is
Option A:	div $\bar{a}$=0 , curl $\bar{a}$=5
Option B:	div $\bar{a}$=2 , curl $\bar{a}$=0
Option C:	div $\bar{a}$=3 , curl $\bar{a}$=3
Option D:	div $\bar{a}$=0 , curl $\bar{a}$=0
19.	If the vector $\vec{F} = (x + 2y + az)i + (bx - 3y - z)j + (4x + cy + 2z)k$ is irrotational; find the constants a, b, c.
Option A:	a=1, b=2, c=4
Option B:	a=-1, b=4, c=2
Option C:	a=4, b=2, c=1
Option D:	a=4, b=2, c=-1
20.	Evaluate $\int_C ydx + xdy$ along $y = x$ from A(0,0) to B(1,1)
Option A:	1
Option B:	2xy
Option C:	-1
Option D:	0

Q2. **(20 Marks Each)**	**Solve any Four out of Six** **5 marks each**
A	*Find* $L\left\{\int_0^t e^{2u}\cos^2 u\,du\right\}$
B	$L^{-1}\left\{\tan^{-1}\left(\frac{2}{s^2}\right)\right\}$
C	*Obtain the Fourier series for* $f(x) = x$ *in* $(0,2\pi)$
D	*Find the analytic function* $f(z)$ *whose real part is* $\frac{1}{2}\log(x^2 + y^2)$
E	*Show that* $A = \begin{vmatrix} 1 & 2 & 3 \\ 2 & -1 & 4 \\ 3 & 1 & -1 \end{vmatrix}$ *satisfies Cayley-Hamilton theorem. Hence*

	find A^{-1}
F	Evaluate by using Green's theorem $\int_C (3x^2 - 8y^2)dx + (4y - 6xy)dy$, where C is the closed region bounded $by\ y = \sqrt{x}$ and $y = x^2$

Q3. **(20 Marks Each)**	**Solve any Four out of Six** **5 marks each**
A	*Evaluate* $\int_0^{\infty} e^{-t}\left(\frac{\cos 3t - \cos t}{t}\right) dt$
B	*Find the inverse Laplace transform by using convolution theorem* $\frac{s+3}{(s^2+6s+13)^2}$
C	*Obtain the half range Fourier cosine series expansion for* $f(x) = x(2 - x)$ *in* $(0,2)$
D	*Obtain the orthogonal trajectories for the family of curves* $e^{-x}\cos y = C$.
E	*Find the eigen values and eigen vector for* $A = \begin{vmatrix} -2 & 2 & -3 \\ 2 & 1 & -6 \\ -1 & -2 & 0 \end{vmatrix}$
F	Show that $\bar{F} = (y^2 - z^2 + 3yz - 2x)\bar{i} + (3xz + 2xy)\bar{j} + (3xy - 2xz + 2z)\bar{k}$ is both irrotational and solenoidal.

University of Mumbai

Examination 2021 under cluster __(Lead College: _____)

Examinations Commencing from 15th June 2021 to 24th June 2021

Program: **BE Electronics & Telecommunication Engineering**

Curriculum Scheme: Rev 2019 'C' Scheme

Examination: SE Semester III

Course Code: **ECC301** and Course Name: **Engineering Mathematics III**

Time: 2 hour Max. Marks: 80

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Question Number	Correct Option (Enter either 'A' or 'B' or 'C' or 'D')
Q1.	D
Q2.	B
Q3.	A
Q4	C
Q5	A
Q6	B
Q7	D
Q8.	B
Q9.	A
Q10.	D
Q11.	C
Q12.	D
Q13.	C
Q14.	A
Q15.	B
Q16.	B
Q17.	D
Q18.	D
Q19.	D
Q20.	A

University of Mumbai

Examination June 2021

Examinations Commencing from 15th June 2021 to 26th June 2021

Program: **Electronics and Telecommunication Engineering**

Curriculum Scheme: Rev-2019

Examination: SE Semester III

Course Code: ECC304 and Course Name: Network Theory

Time: 2 Hour Max. Marks: 80

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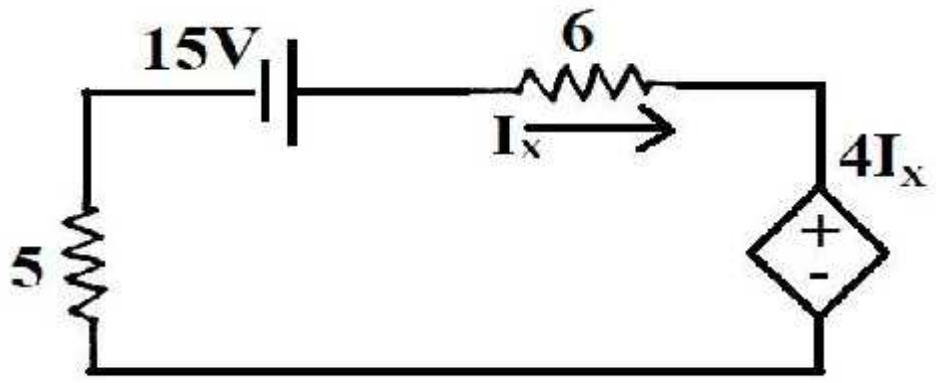
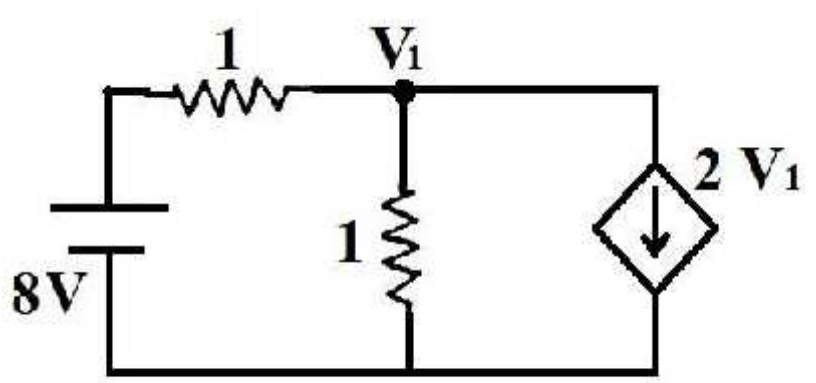
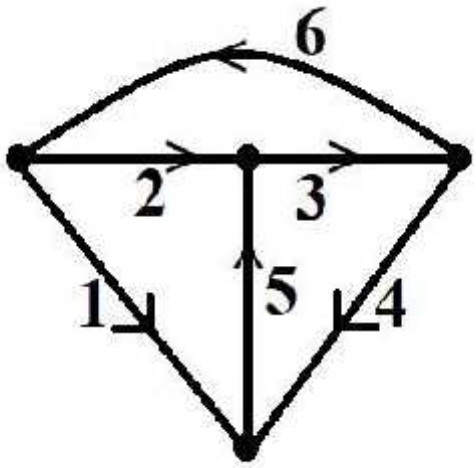
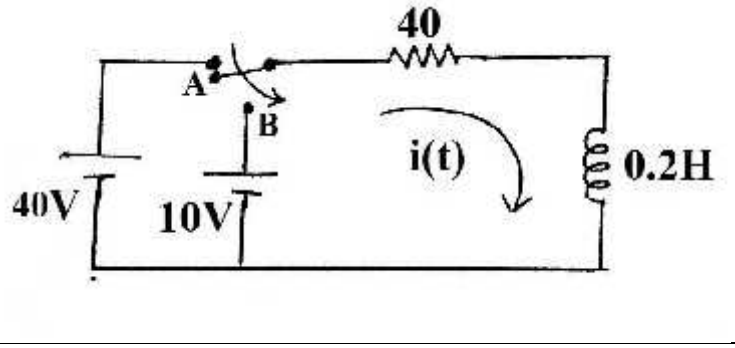
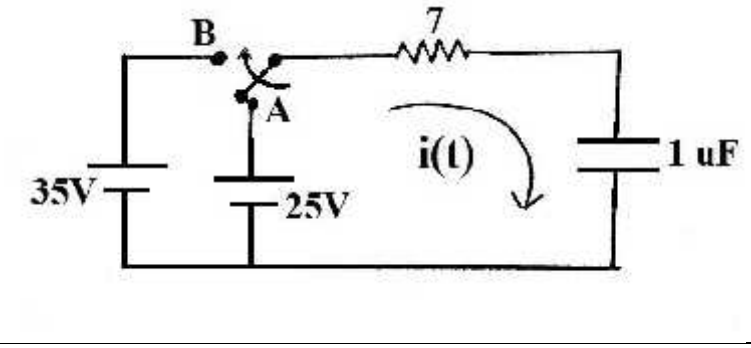
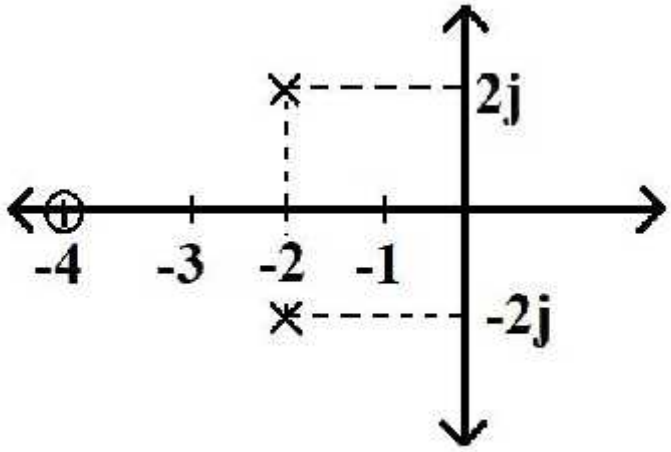
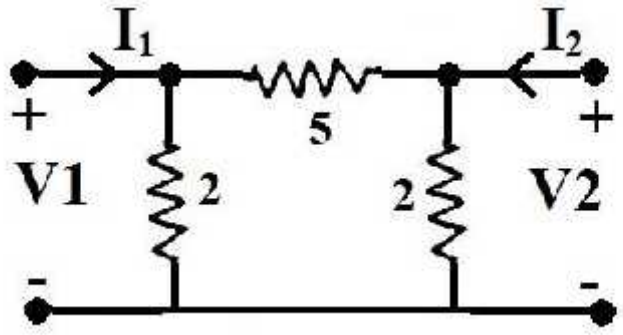
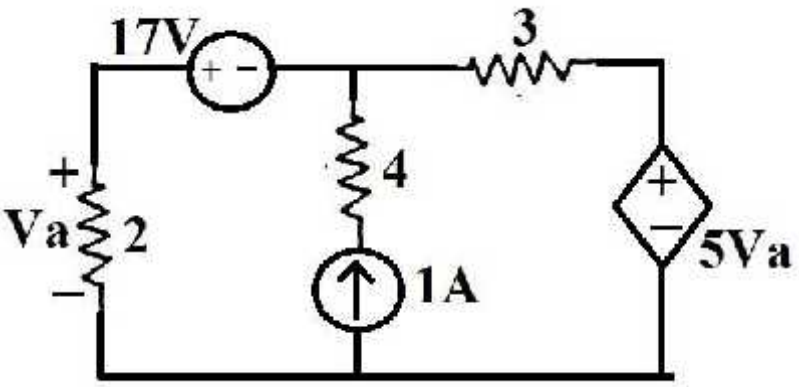
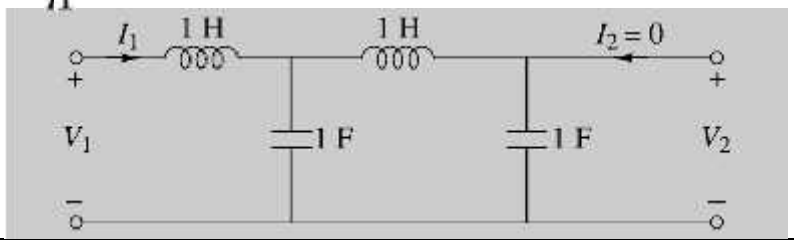
Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks.**
1.	In which theorem equivalent circuit is shown with parallel combination of current source, equivalent resistor and Load?
Option A:	Norton's Theorem
Option B:	Superposition Theorem
Option C:	Maximum power transfer theorem
Option D:	Thevenin's theorem
2.	Coil L1 and L2 are inductively coupled and connected in series with value 16mH and 4mH respectively. If the coefficient of coupling is 0.75, calculate mutual inductance (M).
Option A:	8 mH
Option B:	12 mH
Option C:	6 mH
Option D:	10 mH
3.	In the following figure calculate loop current (Ix). 
Option A:	1 A
Option B:	5 A
Option C:	6 A
Option D:	4 A
4.	Refer the following figure to determine node voltage V1.

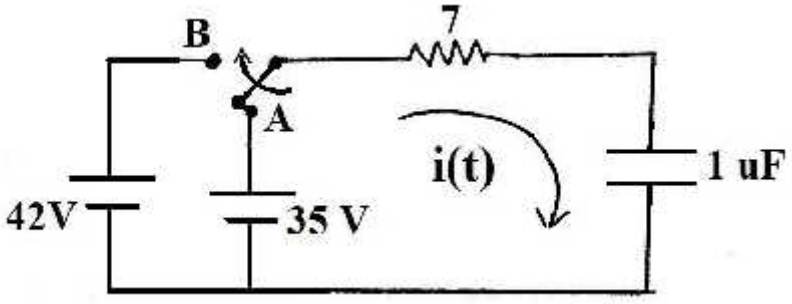
	
Option A:	4 V
Option B:	1 V
Option C:	3.2 V
Option D:	2 V
5.	If the graph consists of 5 nodes and 8 branches then the number of twigs and number of links are ------ and ------ respectively.
Option A:	5, 8
Option B:	6, 3
Option C:	5, 3
Option D:	4, 4
6.	The graph shown in figure, number of rows in reduced incidence matrix are ------- 
Option A:	5
Option B:	4
Option C:	3
Option D:	6
7.	Number of maximum possible trees for the graph is given by --------.
Option A:	N -1
Option B:	b – (n+1)
Option C:	b + n -1
Option D:	$\| A A^T \|$

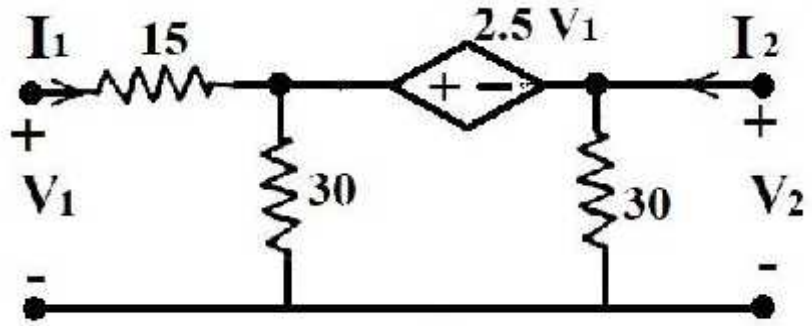
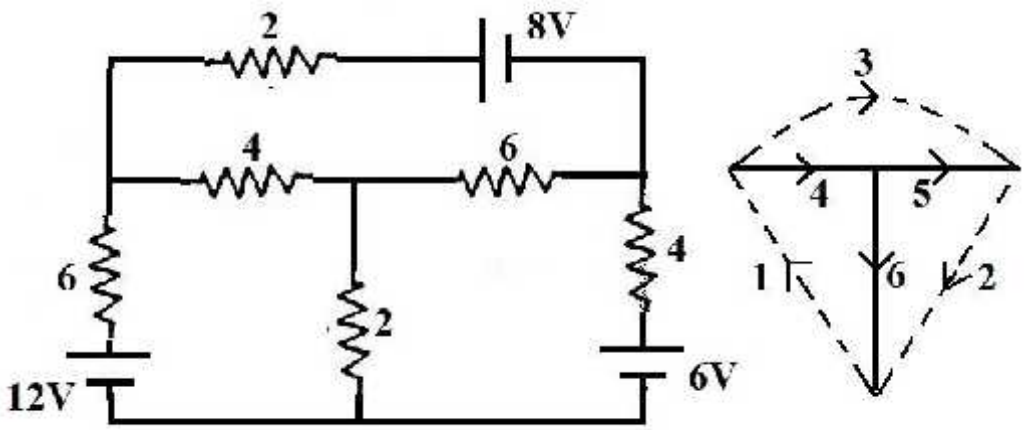
8.	The Laplace transform of the time function *f*(t-a) is --------.
Option A:	$e^{-as}F(S)$
Option B:	F(S-a)
Option C:	$e^{as}F(S)$
Option D:	F(S+a)
9.	In a given network, the switch is at position A for a long time and moved to position B at t=0. Current in the inductor at t=0+ is equal to --------. 
Option A:	8 A
Option B:	0.25 A
Option C:	1 A
Option D:	1.25 A
10.	In the network shown in figure, switch is at position A for a long time and moved to position B at t=0. Voltage across the capacitor at t = 0+ is equal to --------. 
Option A:	3.5 V
Option B:	35 V
Option C:	5 V
Option D:	25 V
11.	Convert R, L and C into S domain.
Option A:	R, L and C
Option B:	RS, LS and CS
Option C:	R, LS and 1/CS
Option D:	R, 1/LS and CS
12.	A system is represented by transfer function 12/(S+4)(S+2), the DC gain of the system is --------.
Option A:	21
Option B:	14
Option C:	1.5

Option D:	294
13.	The driving point impedance function Z(S) of a network has pole-zero location shown in figure, then Z(S) is given by --------. 
Option A:	$\frac{H\ (S+4)}{(S+2-2j)(S+2+2j)}$
Option B:	$\frac{H\ (S-4)}{(S-2-2j)(S-2+2j)}$
Option C:	$\frac{H\ (S-4)}{(S+2-2j)(S+2+2j)}$
Option D:	$\frac{H\ (S+4)}{(S+2-2j)(S-2-2j)}$
14.	Number of poles in the following functions are -----. $F(S) = \frac{S^3+6S^2+4S+5}{S^4+6S^3+3S^2+5S+1}$
Option A:	1
Option B:	3
Option C:	2
Option D:	4
15.	Two 2 port networks are connected in cascade. The combination is to be represented as a single two-port network. The parameters obtained by multiplying individual are ----
Option A:	Z-parameter
Option B:	Y-parameter
Option C:	h-parameter
Option D:	ABCD-parameter
16.	Determine Y11 and Y12 parameters of the network given in figure.

	
Option A:	Y11 = -0.2 □ and Y12 = 0.7 □
Option B:	Y11 = 0.7 □ and Y12 = -0.2 □
Option C:	Y11 = 2 □ and Y12 = 5 □
Option D:	Y11 = 7 □ and Y12 = 2 □
17.	Two port equations of a networks are $V_2 = 8\ I_1 + 7\ I_2$ $V_1 = 3\ I_1 + 5\ I_2$ Z parameters of give network are -------.
Option A:	$Z_{11} = 5,\ Z_{12} = 3, Z_{21} = 7, Z_{22} = 8$
Option B:	$Z_{11} = 3,\ Z_{12} = 5, Z_{21} = 8, Z_{22} = 7$
Option C:	$Z_{11} = 5,\ Z_{12} = 8, Z_{21} = 3, Z_{22} = 7$
Option D:	$Z_{11} = 3,\ Z_{12} = 5, Z_{21} = 7, Z_{22} = 8$
18.	Polynomial $P(S) = S^3 + 4S^2 + 3S + 6$ is to be tested for Hurwitz. Elements in the first column of Routh's array are --------.
Option A:	1, 4, -1.5, 6
Option B:	1, 3, 4, 6
Option C:	1, 4, 3, 6
Option D:	1, 4, 1.5, 6
19.	Driving point admittance function $Y(S) = \frac{14S}{S^2+4}$ is -----.
Option A:	Parallel combination of two resistors
Option B:	Series combination of inductor and resistor
Option C:	Series combination of Inductor and capacitor
Option D:	Parallel combination of Inductor and capacitor
20.	Driving point impedance function Z(S) = 5 + 4s is ----
Option A:	Parallel combination of resistors and inductor.
Option B:	Series combination of resistor and inductor
Option C:	Parallel combination of Capacitor and inductor.
Option D:	Series combination of two inductors

Q2	**Solve any Two Questions out of Three**	**10 marks each**
A	For the circuit shown below, find the current through the 3 ohms resistor, using superposition theorem. 	
B	Synthesize the following driving point impedance function in Cauer-I and Cauer-II forms. $Z(S) = \frac{S^2+4S+3}{S^2+2S}$	
C	Find $\frac{V1}{I1}$, $\frac{V2}{V1}$ and $\frac{V2}{I1}$ for the network shown in figure. 	

Q3	**Solve any Two Questions out of Three**	**10 marks each**
A	In the network shown in figure, switch was at position A for a long time. At t=0, the switch is moved from A to B, determine current i(t) for t>0. 	

B	Find ABCD parameters of the network shown in figure. 
C	Circuit and its tree are shown below. Write tie set matrix and obtain the network equation in matrix form using KVL. Calculate loop current. 

University of Mumbai

Examination June 2021

Examinations Commencing from 15th June 2021 to 26th June 2021

Program: **Electronics and Telecommunication Engineering**

Curriculum Scheme: Rev-2019

Examination: SE Semester III

Course Code: ECC304 and Course Name: Network Theory

Time: 2 hour Max. Marks: 80

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Question Number	Correct Option (Enter either 'A' or 'B' or 'C' or 'D')
Q1.	A
Q2.	C
Q3.	A
Q4	D
Q5	D
Q6	C
Q7	D
Q8.	A
Q9.	C
Q10.	D
Q11.	C
Q12.	C
Q13.	A
Q14.	D
Q15.	D
Q16.	B
Q17.	B
Q18.	D
Q19.	C
Q20.	B

University of Mumbai

Examination June 2021

Examinations Commencing from 15th June 2021 to 26th June 2021

Program: **Bachelor of Engineering**

Curriculum Scheme: **Electronics & Telecommunication (Rev2019 'C' Scheme)**

Examination: **DSE** Semester **III**

Course Code: **ECC304** and Course Name: **Network Theory**

Time: 2-hour Max. Marks: 80

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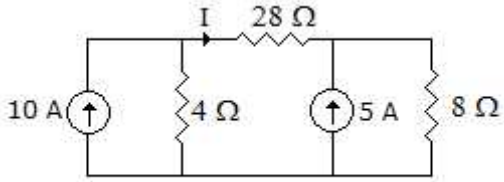
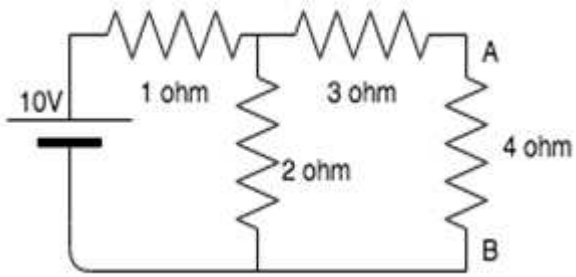
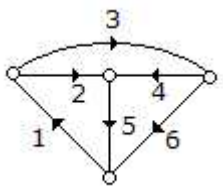
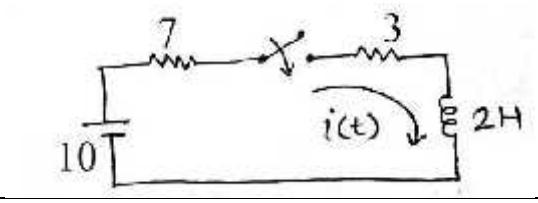
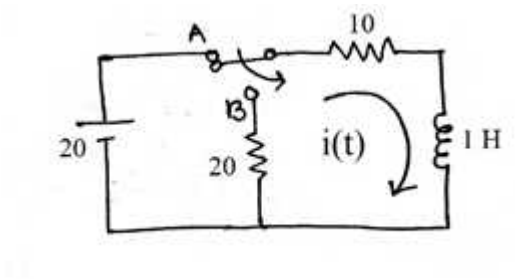
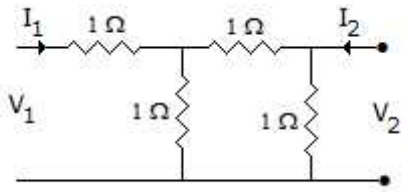
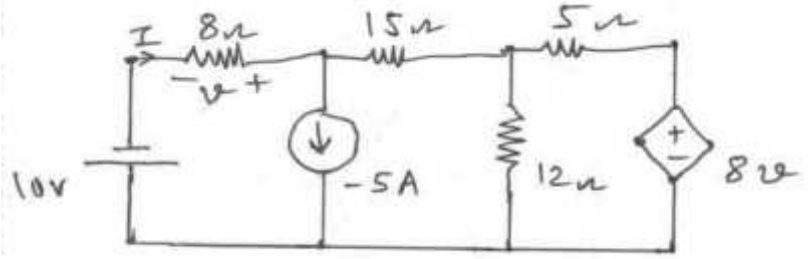
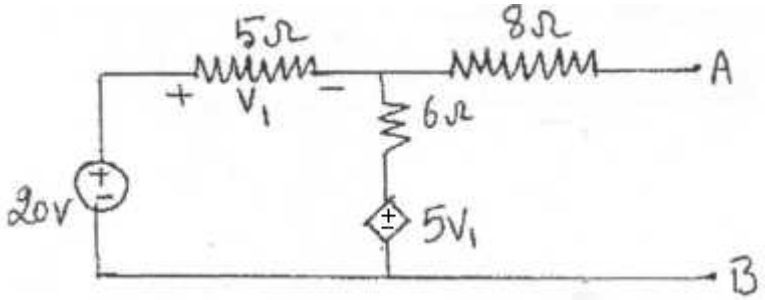
Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks.**
1.	Norton's theorem states that a complex network connected to a load can be replaced with an equivalent impedance
Option A:	in series with a current source
Option B:	in parallel with a voltage source
Option C:	in series with a voltage source
Option D:	in parallel with a current source
2.	Find current I ? 
Option A:	1 A
Option B:	2 A
Option C:	4 A
Option D:	8 A
3.	Determine V_{th} in the following figure. 
Option A:	4.2
Option B:	3.8
Option C:	6.6
Option D:	2.8

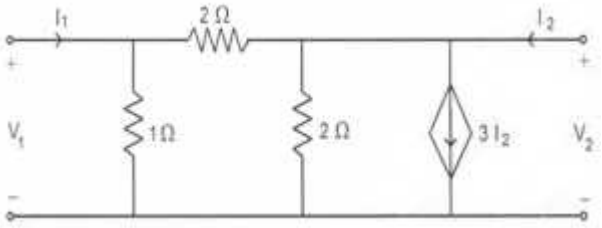
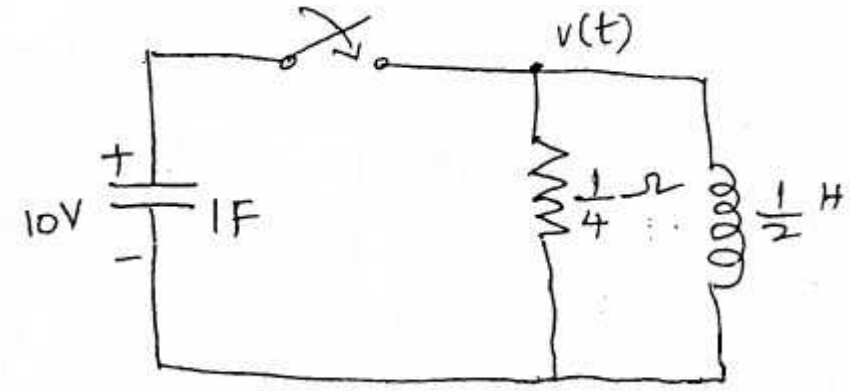
4.	Which one of the following is a cut set of the graph in the given figure? 
Option A:	1, 2, 3, and 4
Option B:	2, 3, 4, and 6
Option C:	1, 4, 5, and 6
Option D:	1, 3, 4, and 5
5.	If 10 V independent voltage source is connected in series with 100 ohm and R_L load. Maximum power that can be transferred to the load is ---
Option A:	5 W
Option B:	10 W
Option C:	0.25 W
Option D:	2.5 W
6.	If a graph consists of 5 nodes and 7 branches, then the number of twigs and number of links are ------ and ------ respectively.
Option A:	3, 4
Option B:	5, 2
Option C:	2, 5
Option D:	4, 3
7.	Reduced Incidence matrix can be obtained by -----
Option A:	Eliminating a row of complete incidence matrix
Option B:	Multiplying complete incidence matrix with its transpose
Option C:	$\| A A^T \|$
Option D:	Obtaining tree
8.	In the following figure, a switch was opened for a long time and then closed at t = 0. Determine i(t) at $t = 0^+$. 
Option A:	1 A
Option B:	0.3 A
Option C:	0.7 A
Option D:	0 A
9.	For an RC driving point impedance function, the poles, and zeros
Option A:	should alternate on real axis
Option B:	should alternate only on negative real axis
Option C:	should alternate on imaginary axis
Option D:	should alternate only on negative imaginary axis

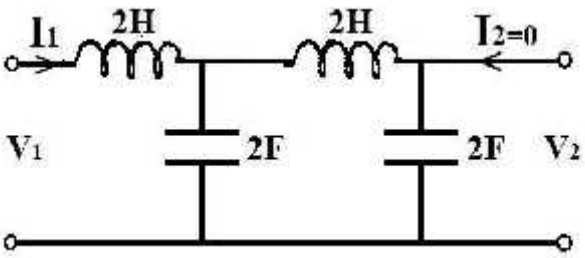
10.	In figure, switch is at position A for long time, what is current at t = 0^-? 
Option A:	20 A
Option B:	3 A
Option C:	1.81 A
Option D:	2 A
11.	Determine location of poles of following transfer function $F(S) = \frac{S^2+1}{S^2+4}$
Option A:	0, 2j
Option B:	1j, -1j
Option C:	-3, -4
Option D:	2j, -2j
12.	For transfer function $(S) = \frac{S+1}{S+7}$ Which of the following is the correct statement?
Option A:	All the poles are at the right half of the S plane.
Option B:	There is a pole at s = -7
Option C:	System has three zeros.
Option D:	There is zero at right half of the S plane
13.	Find out Z_{11}? 
Option A:	5/3 Ohm
Option B:	3/2 Ohm
Option C:	2 Ohm
Option D:	2/3 Ohm
14.	Two port networks are connected in cascade. The combination is to be represented as a single two-port network. The parameters obtained by multiplying individual are ----
Option A:	Z-parameter matrix
Option B:	Y-parameter matrix
Option C:	h-parameter matrix
Option D:	ABCD-parameter matrix

15.	One of the conditions for two port network to be reciprocal is ------
Option A:	$Z_{11} = Z_{22}$
Option B:	$h_{21} = - h_{12}$
Option C:	A = D
Option D:	$Y_{11} = Y_{22}$
16.	Which of the following is the correct generalized KVL equation in graph theory?
Option A:	$B.Z_b.I_l = B.Z_bI_S$
Option B:	$Z_b.B.B^TI_l = B(Z_bI_S - V_S)$
Option C:	$B.Z_b.B^TI_l = B.Vs - B.Z_bI_S$
Option D:	$Y.V_t = Q\ I_S - Q\ Y_b\ Vs$
17.	A Two port network has the following equations. $I2 = 10\ I_1 + 2\ V_2$ and $V_1 = 5\ I_1 + 6\ V_2$ and Hybrid parameters are h_{11}= ------- and h_{12} = -------- respectively.
Option A:	6 and 5
Option B:	10 and 2
Option C:	5 and 6
Option D:	2 and 10
18.	If tree consists of 4 twigs and 3 links, the number of rows in fundamental cutset matrix are ------
Option A:	5
Option B:	4
Option C:	3
Option D:	7
19.	For a series connected R-C network where R = 100 ohm and C = 0.1 uF connected in series. Time constant (τ) of a given circuit is --------.
Option A:	10 uSec
Option B:	1 / 100 Sec
Option C:	100 uSec
Option D:	1 uSec
20.	If a dependent current source has value $8V_1$, where V_1 is voltage across a node in the same circuit, the dependent source represents --------.
Option A:	Current controlled voltage source
Option B:	Voltage controlled current source
Option C:	Voltage controlled voltage source
Option D:	Current controlled current source

Q2	**Solve any Two Questions out of Three** **10 marks each**
A	Find the current I in 8 Ω resistor by using superposition theorem.

	
B	Find Thevenin's equivalent across AB and find the power dissipated in a 25 ohm load. 
C	Draw the graph of the network whose incidence matrix is given below $\begin{bmatrix} 1 & 0 & 1 & 0 & 0 & 0 & 0 & -1 \\ 0 & -1 & 0 & -1 & 0 & -1 & 0 & 0 \\ 0 & 1 & 0 & 0 & 1 & 0 & 0 & 1 \\ 0 & 0 & -1 & 0 & -1 & 0 & 1 & 0 \end{bmatrix}$

Q3.	**Solve any Two Questions out of Three** **10 marks each**
A	Find Z Parameters of the network shown in figure 
B	For the network shown, capacitor C has an initial voltage Vc (-0) of 10 V and at the same instant, current in the inductor L is zero. The switch is closed at time t = 0. Obtain the expression for the voltage V(t) across the inductor L. 
C	Find network function $\frac{V1}{I1}, \frac{V2}{I1}, \frac{V2}{V1}$


I1
2H
2H
I2=0
V1
2F
2F
V2

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Examination June 2021

Examinations Commencing from 15th June 2021 to 26th June 2021

Program: **Bachelor of Engineering**

Curriculum Scheme: **Electronics & Telecommunication (Rev2019 'C' Scheme)**

Examination: **DSE** Semester **III**

Course Code: **ECC304** and Course Name: **Network Theory**

Time: 2 hour Max. Marks: 80

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Question Number	Correct Option (Enter either 'A' or 'B' or 'C' or 'D')
Q1.	D
Q2.	A
Q3.	C
Q4.	D
Q5.	C
Q6.	D
Q7.	A
Q8.	D
Q9.	A
Q10.	D
Q11.	D
Q12.	B
Q13.	A
Q14.	D
Q15.	B
Q16.	C
Q17.	C
Q18.	B
Q19.	A
Q20.	B

University of Mumbai

Examination June 2021

Examinations Commencing from 15th June 2021 to 26th June 2021

Program: **Electronics and Telecommunication**

Curriculum Scheme: Rev2019

Examination: SE Semester III

Course Code: ECC303 and Course Name: Digital System Design

Time: 2 Hour Max. Marks: 80

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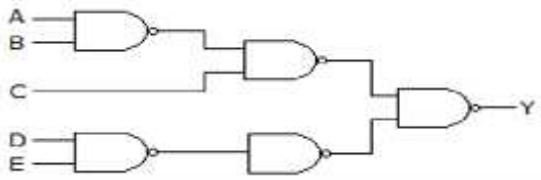
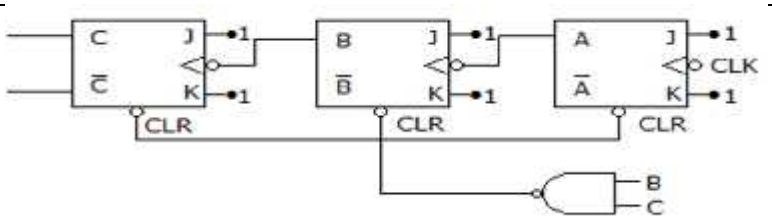
Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	A full adder can be made out of ……
Option A:	two half adders
Option B:	two half adders and a OR gate
Option C:	two half adders and a NOT gate
Option D:	three half adders
2.	The circuit of the given figure realizes the function …… 
Option A:	$Y = (A + B)C + DE$
Option B:	$Y = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D} \cdot \overline{E}$
Option C:	$A(B + (C + D))$
Option D:	$AB + C(D - E)$
3.	What is the hex equivalent of 916, a 4-bit binary number?
Option A:	11112
Option B:	10012
Option C:	01102
Option D:	11002
4.	Which of the following logic families dissipates minimum power ?
Option A:	CMOS
Option B:	ECL
Option C:	TTL
Option D:	DTL
5.	The counter in the given figure is ……

	
Option A:	Mod 3
Option B:	Mod 6
Option C:	Mod 8
Option D:	Mod 7
6.	TTL inputs are the emitters of a _____
Option A:	Transistor-transistor logic
Option B:	Multiple-emitter transistor
Option C:	Resistor-transistor logic
Option D:	Diode-transistor logic
7.	In case of XOR/XNOR simplification, it is required to look for the following: _____
Option A:	Both Diagonal and Straight Adjacencies
Option B:	Only Offset Adjacencies
Option C:	Both Offset and Straight Adjacencies
Option D:	Both Diagonal and Offset Adjacencies
8.	On addition of 28 and 18 using 2's complement, we get _____
Option A:	00101110
Option B:	0101110
Option C:	00101111
Option D:	1001111
9.	One example of the use of an S-R flip-flop is as _____
Option A:	Transition pulse generator
Option B:	Racer
Option C:	Switch debouncer
Option D:	Astable oscillator
10.	If enable input is high then the multiplexer is _____
Option A:	Enable
Option B:	Disable
Option C:	Saturation
Option D:	High Impedance
11.	In D flip-flop, if clock input is LOW, the D input _____
Option A:	Has no effect
Option B:	Goes high
Option C:	Goes low
Option D:	Has effect
12.	Why is a demultiplexer called a data distributor?
Option A:	The input will be distributed to one of the outputs

Option B:	One of the inputs will be selected for the output
Option C:	The output will be distributed to one of the inputs
Option D:	Single input gives single output
13.	The difference between a PAL & a PLA is _____
Option A:	PALs and PLAs are the same thing
Option B:	The PLA has a programmable OR plane and a programmable AND plane, while the PAL only has a programmable AND plane
Option C:	The PAL has a programmable OR plane and a programmable AND plane, while the PLA only has a programmable AND plane
Option D:	The PAL has more possible product terms than the PLA
14.	PROMs are available in _____
Option A:	Bipolar and MOSFET technologies
Option B:	MOSFET and FET technologies
Option C:	FET and bipolar technologies
Option D:	MOS and bipolar technologies
15.	The use of VHDL can be done in _____ ways.
Option A:	2
Option B:	3
Option C:	4
Option D:	5
16.	What is the preset condition for a ring shift counter?
Option A:	All FFs set to 1
Option B:	All FFs cleared to 0
Option C:	A single 0, the rest 1
Option D:	A single 1, the rest 0
17.	In a positive edge triggered JK flip flop, a low J and low K produces?
Option A:	High state
Option B:	Low state
Option C:	Toggle state
Option D:	No Change State
18.	Which is the major functioning responsibility of the multiplexing combinational circuit?
Option A:	Decoding the binary information
Option B:	Generation of all minterms in an output function with OR-gate
Option C:	Generation of selected path between multiple sources and a single destination
Option D:	Encoding of binary information
19.	The octal number (651.124)8 is equivalent to _____
Option A:	(1A9.2A)16
Option B:	(1B0.10)16
Option C:	(1A8.A3)16
Option D:	(1B0.B0)16
20.	The addition of +19 and +43 results as _____ in 2's complement system.

Option A:	11001010
Option B:	101011010
Option C:	00101010
Option D:	0111110

subjective/descriptive questions

Option 1

Q2 **(20 Marks Each)**	**Solve any Four out of Six** **5 marks each**
A	Compare TTL and CMOS Logic Families.
B	Design full adder using 3:8 decoder.
C	Convert (532.125) base 8, into decimal, binary and hexadecimal.
D	VHDL Code for full subtractor.
E	Convert SR Flip Flop to JK Flip Flop.
F	Compare SRAM with DRAM .

Option 2

Q3. **(20 Marks Each)**	**Solve any Two Questions out of Three** **10 marks each**
A	Design 3 bit binary to gray converter.
B	Minimize the following expression using Quine Mc-cluskey technique. $F(A,B,C,D)=\sum M(0,1,2,3,5,7,9,11)$
C	Design Synchronous counter using D-type flip flops for getting the following sequence 0-2-4-6-0.take care of lockout condition.

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Examination June 2021

Examinations Commencing from 15th June 2021 to 26th June 2021

Program: **Electronics & Telecommunication**

Curriculum Scheme: Rev2019

Examination: SE Semester III

Course Code: ECC303 and Course Name: Digital System Design

Time: 2-hour Max. Marks: 80

==========

Question Number	Correct Option (Enter either 'A' or 'B' or 'C' or 'D')
Q1.	B
Q2.	A
Q3.	B
Q4	A
Q5	B
Q6	B
Q7	D
Q8.	B
Q9.	C
Q10.	B
Q11.	A
Q12.	A
Q13.	B
Q14.	D
Q15.	B
Q16.	D
Q17.	D
Q18.	C
Q19.	A
Q20.	D

University of Mumbai

Examination June 2021

Examinations Commencing from 15th June 2021 to 26th June 2021

Program: **Bachelor of Engineering**

Curriculum Scheme: **Electronics & Telecommunication (Rev2019 'C' Scheme)**

Examination: **DSE** Semester **III**

Course Code: **ECC303** and Course Name: **Digital System Design**

Time: 2 hour Max. Marks: 80

==========

Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks.**
1.	Convert binary number into gray code: 100101.
Option A:	101101
Option B:	001110
Option C:	110111
Option D:	111001
2.	The representation of octal number (532.2)8 in decimal is _____
Option A:	(346.25)10
Option B:	(532.864)10
Option C:	(340.67)10
Option D:	(531.668)10
3.	The octal number (651.124)8 is equivalent to _____
Option A:	(1A9.2A)16
Option B:	(1B0.10)16
Option C:	(1A8.A3)16
Option D:	(1B0.B0)16
4.	How many AND gates are required to realize Y = CD + EF + G?
Option A:	4
Option B:	5
Option C:	3
Option D:	2
5.	Which of the following is not a basic gate?
Option A:	AND
Option B:	OR
Option C:	EXOR
Option D:	NOT
6.	A(A + B) = ?
Option A:	AB
Option B:	1
Option C:	(1 + AB)
Option D:	A

7.	A Karnaugh map (K-map) is an abstract form of _____ diagram organized as a matrix of squares.
Option A:	Venn Diagram
Option B:	Cycle Diagram
Option C:	Block diagram
Option D:	Triangular Diagram
8.	Odd parity of word can be conveniently tested by _____
Option A:	OR gate
Option B:	AND gate
Option C:	NAND gate
Option D:	XOR gate
9.	If A and B are the inputs of a half adder, the sum is given by _____
Option A:	A AND B
Option B:	A OR B
Option C:	A XOR B
Option D:	A EX-NOR B
10.	The output of a subtractor is given by (if A, B and X are the inputs).
Option A:	A AND B XOR X
Option B:	A XOR B XOR X
Option C:	A OR B NOR X
Option D:	A NOR B XOR X
11.	The addition of two decimal digits in BCD can be done through _____
Option A:	BCD adder
Option B:	Full adder
Option C:	Ripple carry adder
Option D:	Carry look ahead
12.	Which of the following is correct for a D-type flip-flop?
Option A:	The output follows the D input with each clock pulse.
Option B:	The output complement follows the D input with each clock pulse
Option C:	The output remains HIGH all the time
Option D:	The output toggles with each clock pulse
13.	In a Master Slave flip flop the output is taken
Option A:	from the Master
Option B:	from the Slave
Option C:	from Master output ANDED with Slave output
Option D:	from Master output ORED with Slave output
14.	How can parallel data be taken out of a shift register simultaneously?
Option A:	Use the Q output of the first FF
Option B:	Use the Q output of the last FF
Option C:	Tie all of the Q outputs together
Option D:	Use the Q output of each FF
15.	PLA is used to implement _____

Option A:	A complex sequential circuit
Option B:	A simple sequential circuit
Option C:	A complex combinational circuit
Option D:	A simple combinational circuit
16.	VHDL is being used for _____
Option A:	Documentation only
Option B:	Verification only
Option C:	Synthesis only of digital design
Option D:	Documentation, Verification and Synthesis of digital design
17.	Where do we declare the loop index of a FOR LOOP?
Option A:	Entity
Option B:	Architecture
Option C:	Library
Option D:	It doesn't have to be declared
18.	In delay flip-flop, _____ after the propagation delay.
Option A:	Input follows input
Option B:	Input follows output
Option C:	Output follows input
Option D:	Output follows output
19.	Comparators are used in _____
Option A:	Memory
Option B:	CPU
Option C:	Motherboard
Option D:	Hard drive
20.	A magnitude comparator is defined as a digital comparator which has _____
Option A:	Only one output terminal
Option B:	Two output terminals
Option C:	Three output terminals
Option D:	No output terminal

Q2.	**Answer the following :**
A	**Solve any Two** **5 marks each**
i.	State and prove Demorgan's theorem.
ii.	Compare PAL with PLA .
iii.	Perform the following operation using 2's complement. i) $(14)_{BASE}(10) - (24)_{BASE}(10)$ ii) (24)BASE (10) (14)BASE (10)
B	**Solve any One** **10 marks each**
i.	Minimize the following expression using Quine MC-cluskey technique. $F(A, B, C, D) = \sum M(0,1,2,3,5,7,9,11)$
ii.	Prove that NAND and NOR gates are universal gates.

Q3.	**Answer the following:**
A	**Solve any Two** **5 marks each**

i.	Write the VHDL code for a full subtractor.	
ii.	Convert SR Flip flop to JK Flip flop.	
iii.	Design 3 bit full adder circuit and explain in detail.	
B	**Solve any One**	**10 marks each**
i.	What are shift registers? How are they classified? Explain working of any type of shift register.	
ii.	Draw and explain a neat circuit diagram of BCD adder .	

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Examination June 2021

Examinations Commencing from 15th June 2021 to 26th June 2021

Program: **Bachelor of Engineering**

Curriculum Scheme: **Electronics & Telecommunication (Rev2019 'C' Scheme)**

Examination: **DSE** Semester **III**

Course Code: **ECC303** and Course Name: **Digital System Design**

Time: 2 hour Max. Marks: 80

==========

Question Number	Correct Option (Enter either 'A' or 'B' or 'C' or 'D')
Q1.	C
Q2.	A
Q3.	A
Q4.	D
Q5.	C
Q6.	D
Q7.	A
Q8.	D
Q9.	C
Q10.	B
Q11.	A
Q12.	A
Q13.	B
Q14.	D
Q15.	C
Q16.	D
Q17.	D
Q18.	C
Q19.	B
Q20.	C

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Examination June 2021

Examinations Commencing from 15th June 2021 to 26th June 2021

Program: Electronics and Telecommunication Engineering

Curriculum Scheme: Rev 2019

Examination: SE, Semester: III

Course Code: ECC302 and Course Name: Electronic Devices and Circuits

Time: 2 Hour Max. Marks: 80

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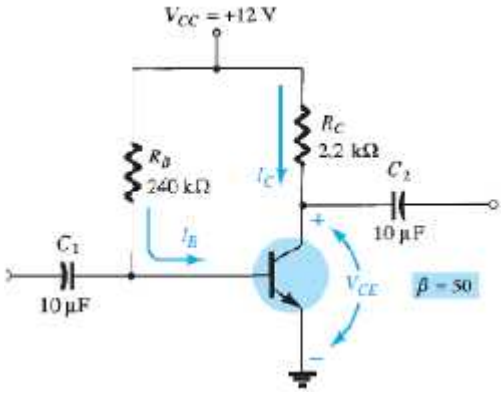
Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	For Zener diode as a voltage regulator , load regulation means _____
Option A:	variable input voltage and fixed load resistor
Option B:	variable input voltage and variable load resistor
Option C:	fixed input voltage and variable load resistor
Option D:	fixed input voltage and fixed load resistor
2.	As an Amplifier BJT should be used in _____ region.
Option A:	Cut-off
Option B:	Saturation
Option C:	Breakdown
Option D:	Active
3.	As an Amplifier MOSFET should be used in _____ region.
Option A:	Cut-off
Option B:	Saturation
Option C:	Breakdown
Option D:	linear
4.	In BJT according to higher to lower doping concentration sequence is _____
Option A:	base,emitter and collector
Option B:	emitter, collector and base
Option C:	collector,base and emitter
Option D:	Emitter, base and collector
5.	In BJT for Active region _____ junction should be forward bias and _____ junction should be reverse bias
Option A:	BE, CB
Option B:	CB, BE
Option C:	BE, EB
Option D:	CE, BE

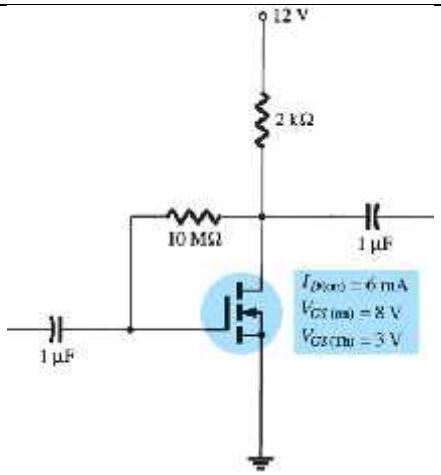
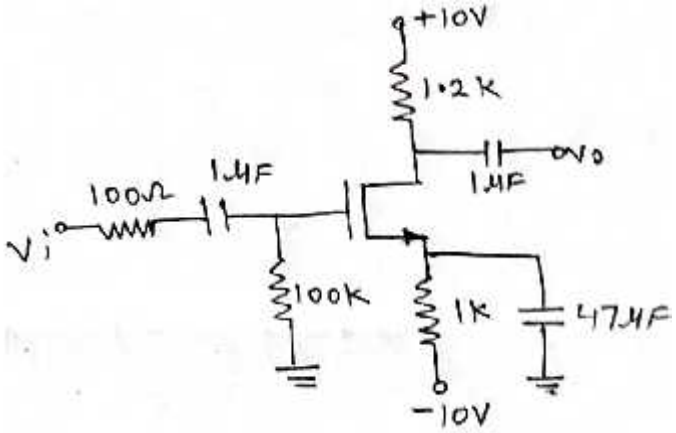
6.	In BJT biasing circuits VBE decreases about _____per degree celsius(°C) increase in temperature.
Option A:	25mV
Option B:	2.5mV
Option C:	2.5V
Option D:	25V
7.	ICO (reverse saturation current) _____ in value for every 10°C increase in temperature
Option A:	triples
Option B:	remains same
Option C:	zero
Option D:	doubles
8.	Which among the below mentioned implementation strategies is/are precise to obtain an AC equivalent circuit of MOSFET? A. Replacement of all capacitors by open circuits B. Replacement of all capacitors by short circuits C. Setting of all DC voltages to zero D. Setting of all DC voltages to unity
Option A:	A & C
Option B:	B & C
Option C:	B & D
Option D:	A & D
9.	The E-MOSFET drain feedback CS amplifier with the result that rd = 50 k, RF = 10M, RD = 2.2 K, gm = 1.75 mS, find the output impedance?
Option A:	49.75 k
Option B:	2.11 k
Option C:	50 k
Option D:	10 M
10.	When a multistage amplifier is to amplify low frequency signal, then one must use …….. coupling
Option A:	RC
Option B:	Transformer
Option C:	Direct
Option D:	impedance
11.	In a multistage amplifier, the overall frequency response is determined by the
Option A:	Frequency response of each stage depending on the relationships of the critical frequencies.
Option B:	frequency response of the first amplifier

Option C:	frequency response of the last amplifier
Option D:	lower critical frequency of the first amplifier and the upper critical frequency of the final amplifier
12.	In the mid frequency region, coupling capacitor acts as a _____ circuits and stray capacitance acts as a _____ circuits
Option A:	open, short
Option B:	short, open
Option C:	short, short
Option D:	open, open
13.	The _____ of the two values of higher cutoff frequencies is the dominant frequency of complete system
Option A:	highest
Option B:	lowest
Option C:	middle
Option D:	average
14.	Which BJT transistor has a better high frequency response?
Option A:	NPN
Option B:	PNP
Option C:	Neither NPN nor PNP
Option D:	Frequency response doesn't depend on type of BJT
15.	The size of a power transistor is made considerably large to ……
Option A:	Provide easy handling
Option B:	Dissipate heat
Option C:	Facilitate connections
Option D:	Consume heat
16.	The main disadvantage of class B type push-pull power amplifier is
Option A:	Harmonic distortion
Option B:	Aliasing problem
Option C:	Crossover distortion
Option D:	Two transistor required
17.	If differential mode gain is 3500 and common mode gain is 3.5, the CMRR is _____
Option A:	1000
Option B:	0.001
Option C:	12250
Option D:	3503.5
18.	CMRR of a differential amplifier can be improved by decreasing _____

Option A:	Differential voltage gain
Option B:	Common mode voltage gain
Option C:	Supply current
Option D:	Supply voltage
19.	When a differential amplifier is operated single-ended, ……
Option A:	The output is grounded
Option B:	One input is grounded and signal is applied to the other
Option C:	Both inputs are connected together
Option D:	The output is not inverted
20.	In the common mode, ……
Option A:	Both inputs are grounded
Option B:	The outputs are connected together
Option C:	An identical signal appears on both the inputs
Option D:	The output signal are in-phase

Q2	**Solve any Two Questions out of Three 10 marks each**
A	Draw high frequency equivalent circuit of MOSFET CS amplifier with Rs unbypassed and self bias. Derive the expression for input and output upper cutoff frequencies with considering input signal resistor (Rsig) and load resistor (R_L).
B	Explain class-AB push pull amplifier in detail?
C	Find the Q point for the following circuit Fig. 1, and also determine the voltage gain, input impedance and output impedance  Fig. 1

Q3.	
A	**Solve any Two 5 marks each**
i.	Explain Zener diode as a voltage regulator
ii.	Explain construction and working of n-channel E-MOSFET
iii.	Find the Q point for the following circuit Fig. 2

	 Fig. 2
B	**Solve any One 10 marks each**
i.	For the circuit shown in Fig. 3, Transistor parameters are Kn = 1 mA/V^2, Vtn = 0.7 V, Cgs = 2 pF, Cgd = 0.2 pF, λ = 0, find the mid band voltage gain, miller capacitance and upper cut-off frequency.  Fig. 3
ii.	Derive the equation of CMRR for the MOS differential pair amplifier.

University of Mumbai

Examination June 2021

Examinations Commencing from 15th June 2021 to 26th June 2021

Program: **Bachelor of Engineering**

Curriculum Scheme: **Electronics & Telecommunication (Rev2019 'C' Scheme)**

Examination: **DSE** Semester **III**

Course Code: **ECC302** and Course Name: **Electronic Devices & Circuits**

Time: 2 hour Max. Marks: 80

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Question Number	Correct Option (Enter either 'A' or 'B' or 'C' or 'D')
Q1.	A
Q2.	A
Q3.	C
Q4.	D
Q5.	A
Q6.	A
Q7.	A
Q8.	A
Q9.	A
Q10.	D
Q11.	C
Q12.	D
Q13.	A
Q14.	B
Q15.	D
Q16.	A
Q17.	A
Q18.	D
Q19.	C
Q20.	B

University of Mumbai

Examination June 2021

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Program: **Bachelor of Engineering**

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Time: 2 hour Max. Marks: 80

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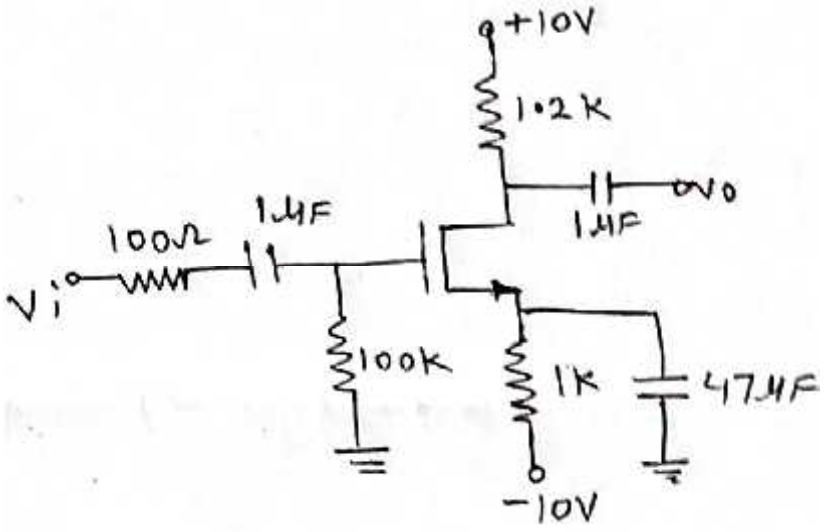
Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	In AC load line, slope is generally
Option A:	Greater than slope of DC load line
Option B:	Less than slope of DC load line
Option C:	Same as that of DC load line
Option D:	Greater than as well as less than slope of DC load line
2.	In AC load line ,the slope is represented by an equation is
Option A:	Y = -1 / Rac
Option B:	Y = 1 / Rac
Option C:	Y = -1 / RL
Option D:	Y = 1 / RL
3.	A transistor with β = 120 is biased to operate at a dc collector current of 1.2 mA. Find the value of rπ.
Option A:	2.2 KΩ
Option B:	2.35 KΩ
Option C:	2.5 KΩ
Option D:	2.45 KΩ
4.	The SI units of transconductance is
Option A:	Volt/ Ampere
Option B:	Ohm
Option C:	Siemens
Option D:	Ampere/ Volt
5.	The enhancement MOSFET is
Option A:	Normally open MOSFET
Option B:	Useful as a very good constant voltage source
Option C:	Widely used because of easy in its fabrication
Option D:	Normally close MOSFET
6.	A CS amplifier has a voltage gain of
Option A:	$g_m (r_d \| \| R_D)$
Option B:	$g_m r_d$
Option C:	gm Rs

Option D:	gm rs / (1+gm rs)
7.	For which of the following frequency region(s) can the coupling and bypass capacitors no longer be replaced by the short-circuit approximation?
Option A:	Low-frequency
Option B:	Mid-frequency
Option C:	High-frequency
Option D:	All frequency
8.	What is the normalized gain expressed in dB for the cut-off frequencies?
Option A:	–3 dB
Option B:	+3 dB
Option C:	–6 dB
Option D:	–20 dB
9.	The larger capacitive elements of the design will determine the _____ frequency.
Option A:	Lower cut off
Option B:	Middle
Option C:	Higher cut off
Option D:	Intermediate
10.	What is the ratio of the capacitive reactance XCS to the input resistance Ri of the input RC circuit of a single-stage BJT amplifier at the low-frequency cut-off?
Option A:	0.25
Option B:	0.50
Option C:	0.75
Option D:	1.0
11.	Which of the lower cutoff -frequency determined by Cin, Cout, and CE will be the predominant factor in determining the low-frequency response for the complete system?
Option A:	Lowest
Option B:	Middle
Option C:	Highest
Option D:	Average
12.	Which of the following elements is (are) important in determining the gain of the system in the high-frequency region?
Option A:	Coupling capacitances
Option B:	Bypass capacitances
Option C:	Transconductance
Option D:	Inter-electrode, wiring and miller effect capacitances
13.	In a multistage amplifier, the overall frequency response is determined by the
Option A:	Frequency response of each stage depending on the relationships of the critical frequencies.
Option B:	Frequency response of the first amplifier.
Option C:	Frequency response of the last amplifier.

Option D:	Lower critical frequency of the first amplifier and the upper critical frequency of the final amplifier.
14.	In the mid frequency region, coupling capacitor acts as a _____ circuits and stray capacitance acts as a _____ circuits.
Option A:	Open, Short
Option B:	Short, Open
Option C:	Short, Short
Option D:	Open, Open
15.	Differential Amplifier amplifies
Option A:	Input signal with higher voltage
Option B:	Input voltage with smaller voltage
Option C:	Sum of the input voltage
Option D:	Difference between the input voltage
16.	If output is measured between two collectors of transistors, then the Differential amplifier with two input signal is said to be configured as
Option A:	Dual Input Balanced Output
Option B:	Dual Input Unbalanced Output
Option C:	Single Input Balanced Output
Option D:	Single Input Unbalanced Output
17.	To increase the value of CMRR, which circuit is used to replace the emitter resistance R_E in differential amplifiers?
Option A:	Constant current bias
Option B:	Resistor in parallel with R_E
Option C:	Resistor in series with R_E
Option D:	Diode in parallel with R_E
18.	The input stage of an op amp is usually a
Option A:	Swamped amplifier
Option B:	Class B push-pull amplifier
Option C:	CE amplifier
Option D:	Differential amplifier
19.	Class _____power amplifier has highest collector efficiency
Option A:	A
Option B:	B
Option C:	C
Option D:	AB
20.	The maximum efficiency of transformer coupled class A power amplifier is _____
Option A:	78.5 %
Option B:	50%
Option C:	30%
Option D:	25%

Q2	**Solve any Two Questions out of Three** **10 marks each**
A	Explain the concept of multistage amplifier with advantage, disadvantage and application.
B	For the circuit shown in Fig. 1, Transistor parameters are Kn = 1 mA/V^2, Vtn = 0.7 V, Cgs = 2 pF, Cgd = 0.2 pF, λ = 0, find the mid band voltage gain, miller capacitance and upper cut-off frequency.  Fig.1
C	Draw a small signal equivalent structure of Diff-amp and derive the equation for its CMRR.

Q3.	**Solve any Two Questions out of Three** **10 marks each**
A	Derive the equation of Av, Zi and Zo of CE amplifier using un-bypass R_E.
B	Explain the effects of coupling, bypass capacitor and parasitic capacitor on frequency response of single stage amplifier.
C	Draw a neat diagram of a transformer coupled Class A power amplifier and explain its working, hence find its efficiency.

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Examination June 2021

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Program: Electronics and Telecommunication Engineering

Curriculum Scheme: Rev 2019

Examination: SE, Semester: III

Course Code: ECC302 and Course Name: Electronic Devices and Circuits

Time: 2 hour Max. Marks: 80

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Question Number	Correct Option (Enter either 'A' or 'B' or 'C' or 'D')
Q1.	C
Q2.	D
Q3.	B
Q4	B
Q5	A
Q6	B
Q7	D
Q8.	A
Q9.	B
Q10.	C
Q11.	A
Q12.	B
Q13.	B
Q14.	A
Q15.	B
Q16.	C
Q17.	A
Q18.	B
Q19.	B
Q20.	C