#### Examinations Commencing from 7th January 2021 to 20th January 2021

#### Program: BE Electronics and Telecommunication Engineering

Curriculum Scheme: Rev 2019 'C' Scheme Examination: SE Semester III

Course Code: ECC301 and Course Name: Engineering Mathematics III

Time: 2 hour Max. Marks: 80

Note: Q1 carrying 40 marks. Q2 and Q3 are carrying 20 equal marks.

| Q1.       | Choose the correct option for following questions. All the Questions are compulsory and carry equal marks  |
|-----------|--|
|           | The second secon |
| 1.        | Find Laplace transform of $f(t) = 1$ , $0 < t < 5$ ; $f(t) = 0$ , $t > 0$  |
| Option A: | 1_ a-5s  |
| Option B: | $\frac{1}{s}e^{-5s}$ $\frac{1}{s}e^{-5s}$  |
| Option C: | 1<br>-<br>s  |
| Option D: | $\frac{1+e^{-5s}}{s}$  |
|           |  |
| 2.        | If $L[f(t)] = log(\frac{s+3}{s+1})$ , find $L[f(2t)]$  |
| Option A: | $2 \log \left(\frac{s+3}{s+1}\right)$  |
| Option B: | $2 \log \left(\frac{s+6}{s+2}\right)$  |
| Option C: | $\frac{1}{2}log\left(\frac{s+3}{s+1}\right)$   |
| Option D: | $\frac{1}{2}log\left(\frac{s+6}{s+1}\right)$   |
|           |  |
| 3.        | Find $L[te^{-3t}sint]$   |
| Option A: | $\frac{2s-6}{(s^2-6s+10)^2}$   |
| Option B: | $\frac{2s+6}{(s^2+6s+10)^2}$   |
| Option C: | $\frac{1}{(s+3)^2+1}$  |
| Option D: | $\frac{1}{(s^2-6s+10)^2}$  |
|           |  |
| 4.        | Find $L\left[\int_0^t u \sin 3u \ du\right]$   |
| Option A: | $ \begin{array}{c c} \hline 2\\ \hline (s^2+1)^2\\ \hline 2 \end{array} $  |
| Option B: | $(s^2+3)^2$  |
| Option C: | $\frac{6}{(s^2+9)^2}$  |

| Option D:    | 2s  |  |
|--------------|---|--|
| Option D.    | $(s^2+1)^2$   |  |
|              |   |  |
| 5.           | $L^{-1}\left[\frac{s+5}{s^2-25}\right] = ?$   |  |
| Option A:    | $\frac{-\left[s^{2}-25\right]}{\cos 5t+5\sin 5t}$   |  |
| Option B:    | cosh5t + 5 sinh5t   |  |
| Option C:    | cosh5t + sinh5t   |  |
| Option D:    | cosht + 5 sinht   |  |
| o p sous a s |   |  |
| 6.           | Find $L^{-1}\left[\frac{s-2}{s^2-4s+13}\right]$   |  |
| Option A:    | $e^{2t} \frac{\sin 3t}{3}$  |  |
| Option B:    | $e^{-2t} \frac{\sin 3t}{3}$   |  |
| Option C:    | $e^{2t}sin3t$   |  |
| Option D:    | $e^{2t}cos3t$   |  |
| 7.           | In Fourier series of $f(x) = x\cos x$ in $(-\pi, \pi)$ . The value of $a_n$ is  |  |
| Option A:    | 0   |  |
| Option B:    | $\left  \frac{-1}{2} \right $   |  |
| Option C:    | $\frac{2}{\binom{-1}{n}}$   |  |
| Option D:    | $\frac{1}{n^2-1}$   |  |
| 8.           | (2024 77 4 4 4 0  |  |
| 0.           | $f(x) = \begin{cases} \cos x, & -\pi < x < 0 \\ -\cos x, & 0 < x < \pi \text{ is} \end{cases}$  |  |
| Option A:    | Both even and odd function  |  |
| Option B:    | neither even nor odd  |  |
| Option C:    | odd function  |  |
| Option D:    | Even function   |  |
| 9.           | The Fourier series for $f(x)$ in $(0,2\pi)$ is $f(x) = \frac{\pi}{2} - \frac{1}{\pi} \sum_{n=1}^{\infty} \frac{1}{n^2} \cos nx$ .<br>Find the value of $\frac{1}{2\pi} \int_0^{2\pi} [f(x)]^2 dx$ |  |
| Option A:    | $\frac{\pi^3}{4} + \frac{1}{\pi} \sum_{n=1}^{\infty} \frac{1}{n^4}$   |  |
| Option B:    | $\frac{\pi^2}{4} + \frac{1}{2\pi^2} \sum_{n=1}^{\infty} \frac{1}{n^4}$  |  |
| Option C:    | $\frac{\pi^3}{2} - \frac{1}{\pi} \sum_{n=1}^{\infty} \frac{1}{n^4}$   |  |
| Option D:    | 0   |  |
|              |   |  |
| 10.          | A function $f(t)$ is periodic with period $2\pi$ if   |  |

| Option A: | $f(t+2\pi)=0$   |
|-----------|---|
| Option B: | $f(t+2\pi)=2\pi$  |
| Option C: | $f(t+2\pi) = f(2\pi)$   |
| Option D: | $f(t+2\pi) = f(t)$  |
| 1         |   |
| 11.       | Which of the following functions is NOT analytic  |
| Option A: | Sinhz   |
| Option B: | Cosz  |
| Option C: | $ar{z}$   |
| Option D: | $z^2 + z$   |
|           |   |
| 12.       | For $f(z) = u + iv$ analytic, which of the following statement is   |
|           | correct   |
| Option A: | f(z) may satisfy Cauchy-Riemann equation.   |
| Option B: |   |
|           | f(z) is constant function   |
| Option C: | f(z) = 0  |
| Option D: | u, v both are harmonic  |
|           |   |
| 13.       | $\Gamma' = 11$ $1 \cdot 1 \cdot 1$  |
|           | Find k such that $f(z) = \frac{1}{2}\log(x^2 + y^2) + itan^{-1}\frac{kx}{y}$ is analytic  |
| Option A: | K=1   |
| Option B: | K=-1  |
| Option C: | K=0   |
| Option D: | K=2   |
|           |   |
| 14.       | Find the characteristic roots of matrix $A$ ,   |
|           | Where $A = \begin{bmatrix} 3 & -1 & 1 \\ -1 & 5 & -1 \end{bmatrix}$   |
|           | Where $A = \begin{bmatrix} -1 & 3 & -1 \\ 1 & -1 & 3 \end{bmatrix}$   |
| Option A: | $\lambda = 1, 2, 3$   |
| Option B: | $\lambda = 1, 1, -2$  |
| Option C: | $\lambda = 2, 3, 6$   |
| Option D: | $\lambda = -2, -3, -6$  |
|           |   |
| 15.       |   |
|           | $\lambda = 5$ is one of the eigenvalues of $A = \begin{bmatrix} 1 & 2 & 2 \\ 2 & 1 & 2 \\ 2 & 2 & 1 \end{bmatrix}$ . Find the eigenvector corresponding |
|           | to eigenvalue $\lambda = 5$ is  |
| Option A: | [1 - 1 0]'  |
| Option B: | [1 1 1]'  |
| Option C: | [1-1-1]'  |
|           |   |

| Option D: | [1 0 - 1]'  |
|-----------|---|
|           |   |
| 16.       | Γ1 2 ΩI   |
| 10.       | If $A = \begin{bmatrix} 1 & 2 & 8 \\ 0 & -1 & 3 \\ 0 & 0 & 2 \end{bmatrix}$ Find Eigen Values of $A^2 + 3A + 2A^{-1} + I$ |
|           | [0 0 2]   |
| Option A: | 7 2 12  |
| Option B: | 7,-3,12<br>6,-4,11  |
| Option C: | 1,-1,2  |
| Option D: | 7,-3,15   |
|           | -, -, -,  |
| 17.       | If the matrix A has eigen value 1,1,5 then algebraic multiplicity of A for $\lambda = 1$ is                               |
| Option A: | -1  |
| Option B: | 0   |
| Option C: | 1   |
| Option D: | 2   |
|           |   |
| 18.       | The divergence and curl of $\bar{a} = 2i - 3j + k$ is   |
| Option A: | $\operatorname{div} \bar{a}=0$ , $\operatorname{curl} \bar{a}=5$  |
| Option B: | div $\bar{a}$ =2, curl $\bar{a}$ =0   |
| Option C: | div $\bar{a}$ =3, curl $\bar{a}$ =3   |
| Option D: | div $\bar{a}$ =0, curl $\bar{a}$ =0   |
|           |   |
| 19.       | Find the value of a if $\overline{F} = (x - 2z)i + (y - 5x)j + (az + 2x)k$ is solenoidal                                  |
| Option A: | a=2   |
| Option B: | a = -2  |
| Option C: | a = -4  |
| Option D: | a=4   |
| 20.       | Evaluate $\int_C y dx + x dy$ along $y = x^2$ from A(0,0) to B(1,1)   |
| Option A: | 0   |
| Option B: | 2xy   |
| Option C: | -1  |
| Option D: | 1   |

| Q2.             | Solve any Four out of Six   | 5 marks each |
|-----------------|---|--------------|
| (20 Marks Each) |   |              |
| A               | Find $L\left[e^{-t}\int_0^t e^u \cosh u  du\right]$                                   |              |
| В               | $L^{-1}\left[\log\left(1+\frac{4}{s^2}\right)\right]s$                                |              |
| С               | Obtain the Fourier series for $e^{-x}$ in $(0,2\pi)$                                  |              |
| D               | Find the analytic function $f(z)$ whose imaginary part is $e^{-x}(y\sin y + x\cos y)$ |              |

| Е | Show that $A = \begin{bmatrix} 2 & -1 & 1 \\ -1 & 2 & -1 \\ 1 & -1 & 2 \end{bmatrix}$ satisfies Cayley-Hamilton theorem.<br>Hence find $A^{-1}$ |
|---|---|
| F | Evaluate by using Green's theorem $\int_C (x^2 - y) dx + (2y^2 + x) dy$ , where C is the closed region bounded $by y = 4$ and $y = x^2$         |

| Q3.             | Solve any Four out of Six 5 marks each   |
|-----------------|--|
| (20 Marks Each) |  |
| A               | Evaluate $\int_0^\infty e^{-3t} \left( \frac{\sinh t \sin t}{t} \right) dt$  |
| В               | Find $L^{-1} \left[ \frac{S}{(s^2 + 4s + 13)^2} \right]$   |
| С               | Obtain the half range Fourier sine series expansion for $f(x) = (x - x^2)$ in (0,2)  |
| D               | Obtain the orthogonal trajectories for the family of curves $e^{-x} \cos y = C$ .  |
| Е               | Check whether the matrix $A = \begin{bmatrix} 2 & 3 & 4 \\ 0 & 2 & -1 \\ 0 & 0 & 1 \end{bmatrix}$ is diagonalizable        |
| F               | Show that $\overline{F} = (y^2 - z^2 + 3yz - 2x)i + (3xz + 2xy)j + (3xy - 2xz + 2z)k$ is both irrotational and solenoidal. |

#### Examinations Commencing from 7th January 2021 to 20th January 2021

# Program: BE Electronics and Telecommunication Engineering

Curriculum Scheme: Rev 2019 'C' Scheme Examination: SE Semester III

Course Code: ECC301 and Course Name: Engineering Mathematics III

Time: 2 hour Max. Marks: 80

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| Question<br>Number | Correct Option<br>(Enter either 'A' or 'B' |
|--------------------|--|
|                    | or 'C' or 'D')                             |
| Q1.                | A  |
| Q2.                | D  |
| Q3.                | В  |
| Q4                 | С  |
| Q5                 | В  |
| Q6                 | A  |
| Q7                 | A  |
| Q8.                | С  |
| Q9.                | В  |
| Q10.               | D  |
| Q11.               | C  |
| Q12.               | D  |
| Q13.               | В  |
| Q14.               | С  |
| Q15.               | В  |
| Q16.               | A  |
| Q17.               | D  |
| Q18.               | D  |
| Q19.               | В  |
| Q20.               | D  |

#### **Examination 2020 under cluster 5(Lead College: APSIT)**

Examinations Commencing from  $23^{rd}$  December 2020 to  $6^{th}$  January 2021 and from  $7^{th}$  January 2021 to  $20^{th}$  January 2021

Program: Electronics and Telecommunication Engineering

Curriculum Scheme: Rev 2019 Examination: SE, Semester: III

Course Code: ECC302 and Course Name: Electronic Devices and Circuits Time: 2 Hour Max. Marks: 80

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| Q1.       | Choose the correct option for following questions. All the Questions are compulsory and carry equal marks |
|-----------|---|
|           |   |
| 1.        | Cut in voltage for Si and Ge diode is respectively  |
| Option A: | 0.7 V and 0.3 V   |
| Option B: | 0.3 V and 0.7 V   |
| Option C: | 0.5 V and 0.3 V   |
| Option D: | 0.7 V and 0.5 V   |
| 2.        | In forward bias diode current increases   |
| Option A: | linearly  |
| Option B: | exponentially   |
| Option C: | parabolic   |
| Option D: | hyperbolic  |
| 2         |   |
| 3.        | In reverse bias current suddenly increase after   |
| Option A: | breakdown   |
| Option B: | breakover   |
| Option C: | cut in  |
| Option D: | cut out   |
| 4.        | If temperature increases VI characteristics sifts to and if decreases it shifts to                        |
| Option A: | left, right   |
| Option B: | right, left   |
| Option C: | left, remains constant  |
| Option D: | right, remains constant   |
| 5.        | For Zener diode as a voltage regulator , line regulation means  |
| Option A: | fixed input voltage and fixed load resistor   |
| Option B: | variable input voltage and variable load resistor   |
| Option C: | fixed input voltage and variable load resistor  |
| Option D: | variable input voltage and fixed load resistor  |
|           |   |

| 6.        | The value of thermal voltage Vt at room temprature T=300K is calculated by and it is  |
|-----------|---|
| Option A: | KT/q, 26mV  |
| Option B: | KT/q, 28mV  |
| Option C: | q/KT, 26mV  |
| Option D: | q/KT, 28mV  |
|           | -   |
| 7.        | A silicon pn junction at $T = 300$ K has a reverse saturation current of $IS = 2 \times 10 \text{exp}{-}14$ A. Determine the required forward-bias voltage to produce a current of $ID = 1$ mA. |
| Option A: | 641V  |
| Option B: | 6.41V   |
| Option C: | 64.1V   |
| Option D: | 0.641V  |
| 1         |   |
| 8.        | A transistor with $\beta = 120$ is biased to operate at a dc collector current of 1.2 mA.   |
|           | Find the value of $r\pi$ .  |
| Option A: | 625 ohm   |
| Option B: | 1250 ohm  |
| Option C: | 2500 ohm  |
| Option D: | 5000 ohm  |
| 1         |   |
| 9.        | The phase difference between the output and input voltages of a CE amplifier is   |
| Option A: | 180°  |
| Option B: | 0°  |
| Option C: | 90°   |
| Option D: | 270°  |
|           |   |
| 10.       | When a transistor amplifier is operating, the current in any branch is  |
| Option A: | Sum of AC and DC  |
| Option B: | AC only   |
| Option C: | DC only   |
| Option D: | Difference of AC and DC   |
|           |   |
| 11.       | The point of intersection of d.c. and a.c. load lines is called   |
| Option A: | Saturation point  |
| Option B: | Cut off point   |
| Option C: | Operating point   |
| Option D: | Critical point  |
|           |   |
| 12.       | To amplify low frequency signal,is used in multistage amplifiers.   |
| Option A: | RC coupling   |
| Option B: | transformer coupling  |

| Option C: | impedance coupling   |
|-----------|--|
| Option D: | direct coupling  |
|           |  |
| 13.       | Which of the following is the fastest switching device?  |
| Option A: | MOSFET   |
| Option B: | Triode   |
| Option C: | JFET   |
| Option D: | BJT  |
| 1         |  |
| 14.       | Before the invention of power amplifiers for the amplification of audio signals                        |
|           | generally device was used  |
| Option A: | Diode  |
| Option B: | OPAMP  |
| Option C: | Vacuum tubes   |
| Option D: | SCR  |
|           |  |
| 15.       | Power amplifier directly amplifies   |
| Option A: | Voltage of signal but not Current  |
| Option B: | Current of the signal but not Voltage  |
| Option C: | Power of the signal but not Voltage and Current  |
| Option D: | Voltage, Current and Power of the signal   |
|           |  |
| 16.       | In a multistage amplifier, generally the output stage is also called                                   |
| Option A: | Mixer stage  |
| Option B: | Power stage  |
| Option C: | Detector stage   |
| Option D: | Amplifier stage  |
|           |  |
| 17.       | The maximum efficiency of resistance loaded class A power amplifier is                                 |
| Option A: | 5 %  |
| Option B: | 50 %   |
| Option C: | 30 %   |
| Option D: | 25 %   |
|           |  |
| 18.       | The Maximum and minimum output of the Differential amplifiers is defined as:                           |
| Option A: | $Vmax = V_{DD}, Vmin = -V_{DD}$  |
| Option B: | $Vmax = V_{DD}, Vmin = R_D x Iss$  |
| Option C: | $Vmax = V_{DD}$ , $Vmin = V_{DD} - R_D x Iss$  |
| Option D: | $Vmax = -V_{DD}, Vmin = -V_{DD}$   |
|           |  |
| 19.       | In Common Mode Differential Amplifier, the outputs Vout <sub>1</sub> and Vout <sub>2</sub> are related |
|           | as:  |
| Option A: | Vout <sub>2</sub> is in out of phase with Vout <sub>1</sub> with same amplitude.                       |
| Option B: | Vout <sub>2</sub> and Vout <sub>1</sub> have same amplitude but the phase difference is 90 degrees     |

| Option C: | Vout <sub>1</sub> and Vout <sub>2</sub> have same amplitude and are in phase with each other and their  |
|-----------|---|
|           | respective inputs.  |
| Option D: | Vout <sub>1</sub> and Vout <sub>2</sub> have same amplitude and are in phase with each other but out of |
|           | phase with their respective inputs.   |
|           |   |
| 20.       | If output is measured between two collectors of transistors, then the Differential                      |
|           | amplifier with two input signal is said to be configured as   |
| Option A: | Dual Input Balanced Output  |
| Option B: | Dual Input Unbalanced Output  |
| Option C: | Single Input Balanced Output  |
| Option D: | Single Input Unbalanced Output  |

| Q2. | Solve any Two Questions out of Three 10 marks each   |
|-----|--|
| A   | Determine the following for the network given below Fig. 1  Voltage gain, Current gain, input impedance and output impedance $ \begin{array}{cccccccccccccccccccccccccccccccccc$ |
| В   | With neat diagram derive the efficiency of transformer coupled class –A power amplifier? State its uses.   |
| С   | Explain construction and working of n-channel E-MOSFET with output characteristics   |

| Q3.  |   |
|------|---|
| A    | Solve any Two 5 marks each  |
| i.   | Compare BJT and JFET  |
| ii.  | Explain working of pn junction diode with the help of VI characteristics. |
| iii. | Determine the range of values of Vi that will maintain the Zener diode of |
|      | Fig. 2 in the "on" state.   |

|     | $V_{Z} = 20 \text{ V}$ $I_{ZM} = 60 \text{ mA}$ $V_{Z} = R_{L}$ $I_{Z} = R_{L}$ $I_{Z} = R_{L}$ $I_{Z} = R_{L}$  |
|-----|--|
| В   | Solve any One 10 marks each  |
| i.  | For the circuit shown in Fig. 3, the transistor parameter are $V_{BE}$ (on) = 0.7 $V$ , $\beta$ = 200, $VA = \infty$ , i. Derive the expression for lower cutoff frequency due to input coupling capacitor. ii. Determine lower cut-off frequency and voltage gain |
| ii. | Explain the MOS differential pair amplifier with a common-mode input voltage $v_{CM}$ .  |

### **Examination 2020 under cluster 5(Lead College: APSIT)**

Examinations Commencing from 23<sup>rd</sup> December 2020 to 6<sup>th</sup> January 2021 and from 7<sup>th</sup> January 2021 to 20<sup>th</sup> January 2021

Program: Electronics and Telecommunication Engineering

Curriculum Scheme: Rev 2019 Examination: SE, Semester: III

Course Code: ECC302 and Course Name: Electronic Devices and Circuits

Time: 2 hour Max. Marks: 80

| Question<br>Number | Correct Option (Enter either 'A' or 'B' or 'C' or 'D') |
|--------------------|--|
| Q1.                | A  |
| Q2.                | В  |
| Q3.                | A  |
| Q4                 | A  |
| Q5                 | D  |
| Q6                 | A  |
| Q7                 | D  |
| Q8.                | С  |
| Q9.                | A  |
| Q10.               | A  |
| Q11.               | С  |
| Q12.               | D  |
| Q13.               | A  |
| Q14.               | С  |
| Q15.               | D  |
| Q16.               | В  |
| Q17.               | D  |
| Q18.               | С  |
| Q19.               | D  |
| Q20.               | A  |

#### **Examination 2020 under cluster 5 (Lead College: APSIT)**

Examinations Commencing from  $23^{rd}$  December 2020 to  $6^{th}$  January 2021 and from  $7^{th}$  January 2021 to  $20^{th}$  January 2021

#### **Program: Electronics and Telecommunication**

Curriculum Scheme: Rev2019

Examination: SE Semester III

Course Code: ECC303 and Course Name: Digital System Design

Time: 2 Hour Max. Marks: 80

| Q1.       | Choose the correct option for following questions. All the Questions are compulsory and carry equal marks |  |
|-----------|---|--|
| 1         |   |  |
| 1.        | A full adder can be made out of   |  |
| Option A: | two half adders   |  |
| Option B: | two half adders and a OR gate   |  |
| Option C: | two half adders and a NOT gate  |  |
| Option D: | three half adders   |  |
|           |   |  |
| 2.        | POS expressions can be implemented usinglogic circuit.  |  |
| Option A: | 2-level OR-AND  |  |
| Option B: | 2-level OR-AND and NOR  |  |
| Option C: | 2-level XOR   |  |
| Option D: | 2-level NOR   |  |
|           |   |  |
| 3.        | To program basic logic functions which type of PLD should be used?  |  |
| Option A: | PAL   |  |
| Option B: | PLA   |  |
| Option C: | CPLD  |  |
| Option D: | SLD   |  |
|           |   |  |
| 4.        | Sequential structure of VHDL  |  |
| Option A: | Library Declaration; Configuration; Entity Declaration; Architecture Declaration                          |  |
| Option B: | Library Declaration; Entity Declaration; Configuration; Architecture Declaration                          |  |
| Option C: | Library Declaration; Configuration; Architecture Declaration; Entity Declaration                          |  |
| Option D: | Library Declaration; Entity Declaration; Architecture Declaration; Configuration                          |  |
|           |   |  |
| 5.        | VHDL is based on which programming language   |  |
| Option A: | C   |  |
| Option B: | PHP   |  |
| Option C: | Assembly  |  |
| Option D: | ADA   |  |
|           | TTI in most and the smith of a  |  |
| 6.        | TTL inputs are the emitters of a  |  |
| Option A: | Transistor-transistor logic   |  |
| Option B: | Multiple-emitter transistor   |  |
| Option C: | Resistor-transistor logic   |  |
| Option D: | Diode-transistor logic  |  |
|           |   |  |

| 7.        | In case of XOR/XNOR simplification we have to look for the                         |
|-----------|--|
|           | following  |
| Option A: | Both Diagonal and Straight Adjacencies   |
| Option B: | Only Offset Adjacencies  |
| Option C: | Both Offset and Straight Adjacencies   |
| Option D: | Both Diagonal and Offset Adjacencies   |
| •         |  |
| 8.        | On addition of 28 and 18 using 2's complement, we get                              |
| Option A: | 00101110   |
| Option B: | 0101110  |
| Option C: | 00101111   |
| Option D: | 1001111  |
|           |  |
| 9.        | One example of the use of an S-R flip-flop is as                                   |
| Option A: | Transition pulse generator   |
| Option B: | Racer  |
| Option C: | Switch debouncer   |
| Option D: | Astable oscillator   |
|           |  |
| 10.       | Being a universal gate, it is possible for NOR gate to get converted into AND gate |
|           | by inverting the inputs  |
| Option A: | before getting applied to NOR gate   |
| Option B: | after getting applied to NOR gate  |
| Option C: | before getting applied to AND gate   |
| Option D: | after getting applied to AND gate  |
| 11.       | On subtracting (01010)2 from (11110)2 using 1's complement, we get                 |
| Option A: | 01001  |
| Option B: | 11010  |
| Option C: | 10101  |
| Option D: | 10100  |
| opuon 2.  |  |
| 12.       | Which of the following is the most widely employed logic family?                   |
| Option A: | Emitter-coupled logic  |
| Option B: | Transistor-transistor logic  |
| Option C: | CMOS logic family  |
| Option D: | NMOS logic   |
|           |  |
| 13.       | The time required for a gate or inverter to change its state is called             |
| Option A: | Rise time  |
| Option B: | Decay time   |
| Option C: | Propagation time   |
| Option D: | Charging time  |
|           |  |
| 14.       | Internal propagation delay of asynchronous counter is removed by                   |
| Option A: | Ripple counter   |
| Option B: | Ring counter   |
|           | C  |
| Option C: | Modulus counter  |

| 15.       | One of the major drawbacks to the use of asynchronous counters is that  |
|-----------|---|
| Option A: | Low-frequency applications are limited because of internal propagation delays   |
| Option B: | High-frequency applications are limited because of internal propagation delays  |
| Option C: | Asynchronous counters do not have major drawbacks and are suitable for use in high- and low-frequency counting applications |
| Option D: | Asynchronous counters do not have propagation delays, which limits their use in high-frequency applications                 |
| 16.       | What is the preset condition for a ring shift counter?  |
| Option A: | All FFs set to 1  |
| Option B: | All FFs cleared to 0  |
| Option C: | A single 0, the rest 1  |
| Option D: | A single 1, the rest 0  |
| 1         |   |
| 17.       | In a positive edge triggered JK flip flop, a low J and low K produces?  |
| Option A: | High state  |
| Option B: | Low state   |
| Option C: | Toggle state  |
| Option D: | No Change State   |
|           |   |
| 18.       | Which is the major functioning responsibility of the multiplexing combinational circuit?                                    |
| Option A: | Decoding the binary information   |
| Option B: | Generation of all minterms in an output function with OR-gate   |
| Option C: | Generation of selected path between multiple sources and a single destination   |
| Option D: | Encoding of binary information  |
|           |   |
| 19.       | The octal number (651.124)8 is equivalent to  |
| Option A: | (1A9.2A)16  |
| Option B: | (1B0.10)16  |
| Option C: | (1A8.A3)16  |
| Option D: | (1B0.B0)16  |
|           |   |
| 20.       | The addition of +19 and +43 results as in 2's complement system.  |
| Option A: | 11001010  |
| Option B: | 101011010   |
| Option C: | 00101010  |
| Option D: | 0111110   |

# **Subjective/Descriptive Questions**

# Option 1

| Q2               | Solve any Four out of Six 5 marks each                          |
|------------------|---|
| (Total 20 Marks) |   |
| A                | Compare SRAM with DRAM.   |
| В                | Design full adder using 3:8 decoder.                            |
| C                | Convert (532.125) base 8, into decimal, binary and hexadecimal. |
| D                | VHDL Code for full Adder.                                       |
| Е                | Convert JK Flip Flop to T Flip Flop.                            |
| F                | Compare TTL and CMOS Logic Families.                            |

# **Option 2**

| Q3.              | Solve any Two Questions out of Three                       | 10 marks each       |
|------------------|--|---------------------|
| (Total 20 Marks) |  |                     |
| A                | Design 3 bit gray to binary converter.                     |                     |
| D                | Minimize the following expression using Quine Mc-clusk     | ey technique.       |
| В                | $F(A,B,C,D)=\sum M(0,1,2,3,5,7,9,11)$                      |                     |
| С                | Design Synchronous counter using T-type flip flops for get | tting the following |
|                  | sequence 0-2-4-6-0.take care of lockout condition.         |                     |

### **Examination 2020 under cluster 5 (Lead College: APSIT)**

Examinations Commencing from 23<sup>rd</sup> December 2020 to 6<sup>th</sup> January 2021 and from 7<sup>th</sup> January 2021 to 20<sup>th</sup> January 2021

Program: Electronics & Telecommunication

Curriculum Scheme: Rev2019 Examination: SE Semester III

Course Code: ECC303 and Course Name: Digital System Design

Time: 2-hour Max. Marks: 80

| Question<br>Number | Correct Option (Enter either 'A' or 'B' or 'C' or 'D') |
|--------------------|--|
| Q1.                | В  |
| Q2.                | В  |
| Q3.                | A  |
| Q4                 | D  |
| Q5                 | D  |
| Q6                 | В  |
| Q7                 | D  |
| Q8.                | В  |
| Q9.                | С  |
| Q10.               | A  |
| Q11.               | D  |
| Q12.               | В  |
| Q13.               | С  |
| Q14.               | D  |
| Q15.               | В  |
| Q16.               | D  |
| Q17.               | D  |
| Q18.               | С  |
| Q19.               | A  |
| Q20.               | D  |

#### **Examination 2020 under cluster 5 (Lead College: APSIT)**

Examinations Commencing from  $23^{rd}$  December 2020 to  $6^{th}$  January 2021 and from  $7^{th}$  January 2021 to  $20^{th}$  January 2021

Program: Electronics and Telecommunication Engineering

Curriculum Scheme: Rev-2019 Examination: SE Semester III

Course Code: ECC304 and Course Name: Network Theory

Time: 2 Hour Max. Marks: 80

Choose the correct option for following questions. All the Questions are **Q1.** compulsory and carry equal marks Which of the following conditions delivers maximum power to the load? 1. Option A:  $R_L > R_{TH}$ Option B:  $R_L = R_{TH}$  $R_L < R_{TH}$ Option C: Option D: Depends upon source. 2. Determine value of Va shown in the following figure. Option A: 1 V Option B: 2 V Option C: 3 V Option D: 4 V Refer the following figure to find current Ia. 3. 2Ia Option A: 4 A

Option B:

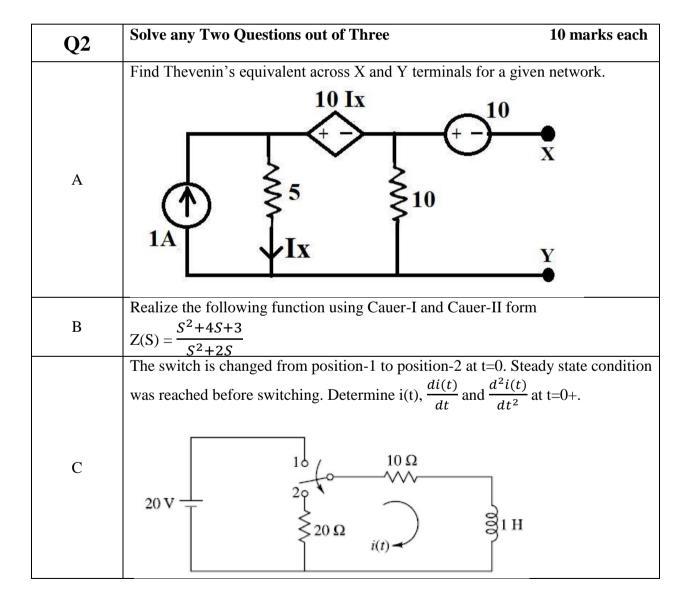
3 A

| Option C:           | 2 A  |
|---------------------|--|
| Option D:           | 1 A  |
|                     |  |
| 4.                  | Two inductively coupled coils are connected in series with the Aiding method, where L1=6mH, L2=6mH and M=1mH. Determine Total inductance of combination. |
| Option A:           | 12 mH  |
| Option B:           | 13 mH  |
| Option C:           | 14 mH  |
| Option D:           | 10 mH  |
| 5.                  | Number of fundamental cutsets in following oriented graphs are   |
|                     | 2 3 5 14   |
| Option A:           | 3  |
| Option B:           | 4  |
| Option C:           | 5  |
| Option D:           | 6  |
| option B.           |  |
| 6.                  | Which of the following is the correct generalized KCL equation in graph theory?  |
| Option A:           | $B.Z_b.B^TI_l = B.Vs - B.Z_bI_S$   |
| Option B:           | $QY_b Q^T \cdot V_t = Q I_S - Q Y_b V_S$   |
| Option C:           | $Y = QY_b Q^T$   |
| Option D:           | $QY_b Q^T \cdot V_t = Q (1 - Q Y_b V_s)$   |
|                     |  |
| 7.                  | Reduced Incidence matrix can be obtained by  |
| Option A:           | Eliminating a row of complete incidence matrix   |
| Option B:           | Multiplying complete incidence matrix with its transpose   |
| Option C:           | $ AA^{T} $   |
| Option D:           |  |
|                     | Obtaining tree   |
| 8.                  | Laplace transform of $\int_0^t f(t) dt$ is equal to  |
| Option A:           | Laplace transform of $\int_0^t f(t) dt$ is equal to d F(S) / dS  |
| Option A: Option B: | Laplace transform of $\int_0^t f(t) dt$ is equal to<br>d F(S) / dS<br>S F(S) – f(0)  |
| Option A:           | Laplace transform of $\int_0^t f(t) dt$ is equal to d F(S) / dS  |

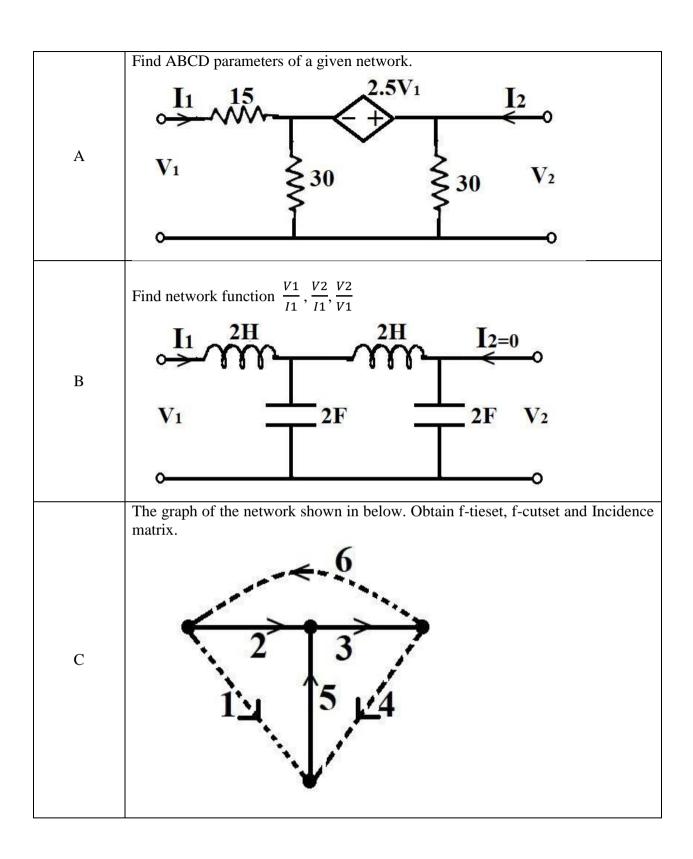
| 9.        | Voltage source V is applied to series connected R and L networks. Equation of the                                    |
|-----------|--|
| ٦.        | current in the inductor is   |
| Ontion A: | Lt   |
| Option A: | $i(t) = V(1 - e^{-\frac{Lt}{R}}) / R$  |
| Option B: | 0  |
| Option C: | $i(t) = V \left(1 - e^{-\frac{Rt}{L}}\right) / R$ $i(t) = \left(e^{-\frac{Rt}{L}}\right)$                            |
| Option D: | $\frac{Rt}{Rt}$  |
| Option B. | $i(t) = (e^{-L})$  |
|           |  |
| 10.       | In the following figure, a switch was opened for a long time and then closed at $t = \frac{1}{2}$                    |
|           | 0. Determine $i(t)$ at $t = 0^+$ .   |
|           | 10T (t) \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \  |
|           |  |
|           | 1(t) & 2H  |
|           | 10T  |
|           |  |
| Option A: | 1 A  |
| Option B: | 0.3 A  |
| Option C: | 0.7 A  |
| Option D: | 0 A  |
| 1.1       |  |
| 11.       | For a series connected R-C network where $R = 100$ ohm and $C = 0.1$ uF connected                                    |
|           | in series. Time constant $(\tau)$ of a given circuit is  |
| Option A: | 10 uSec  |
| Option B: | 1 / 100 Sec  |
| Option C: | 100 <u>u</u> Sec   |
| Option D: | 1 uSec   |
| 12        | The driving point impodence function 7(C) of a network has not a roughly and   |
| 12.       | The driving point impedance function Z(S) of a network has pole-zero location shown in figure, then Z(S) is given by |
|           | shown in figure, then $Z(S)$ is given by   |
|           |  |
|           |  |
|           | T  |
|           | ×3i  |
|           | r S  |
|           | 9  |
|           |  |
|           |  |
|           | -4 -3 -2 -1  |
|           | ×  |
|           | , -J   |
|           |  |
|           | <b>↓</b>   |
| 0         | II (C + 2 - 25)(C + 2 + 25)  |
| Option A: | $\frac{H(S+2-3j)(S+2+3j)}{(S+3)}$  |
| 0 11 5    | $ \begin{array}{c} (S+1) \\ H (S-1) \end{array} $  |
| Option B: |  |
|           | $\overline{(S-2-3j)(S-2+3j)}$  |

| Ontion C: | H(S+1)  |  |  |
|-----------|---|--|--|
| Option C: |   |  |  |
|           | (S+2-3j)(S+2+3j) $H(S+1)$   |  |  |
| Option D: |   |  |  |
|           | $\overline{(S-2-3j)(S-2+3j)}$   |  |  |
|           |   |  |  |
|           |   |  |  |
| 13.       | Polynomial $P(S) = 3S^3 + 4S^2 + 2S + 1$ is to be tested for Hurwitz. Elements in the |  |  |
|           | first column of Routh's array are   |  |  |
| Option A: | 3, 4, 2, 1  |  |  |
| Option B: | 3, 4, -1.25, 1  |  |  |
| Option C: | 3, 4, -2, 1   |  |  |
| Option D: | 3, 4, 1.25, 1   |  |  |
|           |   |  |  |
| 14.       | If inductor and capacitor are connected in series then equivalent impedance is        |  |  |
| Option A: | L+C   |  |  |
| Option B: | LS + 1 / CS   |  |  |
| Option C: |   |  |  |
| 1         | — CS  |  |  |
| Option D: | (S+L)C  |  |  |
| •         |   |  |  |
| 15.       | Two two port networks are connected in parallel. The combination is to be             |  |  |
|           | represented as a single two-port network. The parameters obtained by adding           |  |  |
|           | individuals are   |  |  |
| Option A: | Z-parameter matrix  |  |  |
| Option B: | h-parameter matrix  |  |  |
| Option C: | ABCD-parameter matrix   |  |  |
| Option D: | Y-parameter matrix  |  |  |
|           | •   |  |  |
| 16.       | A Two port network has the following equations.                                       |  |  |
|           | $I2 = 10 I_1 + 2 V_2$ and   |  |  |
|           | $V_1 = 5 I_1 + 6 V_2$ and   |  |  |
|           | Hybrid parameters are $h_{11}$ = and $h_{12}$ = respectively.                         |  |  |
| Option A: | 6 and 5   |  |  |
| Option B: | 10 and 2  |  |  |
| Option C: | 5 and 6   |  |  |
| Option D: | 2 and 10  |  |  |
| *         |   |  |  |
| 17.       | A two port network is said to be symmetrical if                                       |  |  |
| Option A: | Voltage to current ratio at one port is the same as the voltage to current ratio at   |  |  |
| •         | another port with one port open circuited.  |  |  |
| Option B: | Voltage gain and current gain are the same.   |  |  |
| Option C: | Ratio of excitation at one port to response at another port is the same if excitation |  |  |
| 1         | and response is interchanged.   |  |  |
| Option D: | Current gain is same if ports are interchanged  |  |  |
|           |   |  |  |
| 18.       | 3   |  |  |
|           | Driving point impedance function $Z(S) = \frac{S}{S+4}$ is                            |  |  |
| Option A: | Series combination of two inductors   |  |  |
| Option B: | Parallel combination of Inductor and Resistor   |  |  |
| Option C: | Parallel combination of resistor and capacitor  |  |  |
| - r O.    | and expenses  |  |  |

| Option D: | Series combination of two capacitors  |
|-----------|---|
|           |   |
| 19.       | Realization of function using Cauer-II can be obtained by                       |
| Option A: | Partial fraction expansion on Y(S)  |
| Option B: | Partial fraction expansion on Z(S)  |
| Option C: | Division operation on Z(S)  |
| Option D: | Continued fraction expansion  |
|           |   |
| 20.       | Function F(S) = $\frac{(S-3)}{S^2+9S+20}$ is not positive real function because |
| Option A: | A zero is right half of S-Plane   |
| Option B: | Poles are lies on left side of S plane  |
| Option C: | A zero is at left half of S plane   |
| Option D: | All poles lie on left half of S-Plane   |



| 03 | Solve any Two Questions out of Three | 10 marks each |
|----|--------------------------------------|---------------|
| QS |                                      |               |



### **Examination 2020 under cluster 5 (Lead College: APSIT)**

Examinations Commencing from 23<sup>rd</sup> December 2020 to 6<sup>th</sup> January 2021 and from 7<sup>th</sup> January 2021 to 20<sup>th</sup> January 2021

**Program: Electronics and Telecommunication Engineering** 

Curriculum Scheme: Rev-2019 Examination: SE Semester III

Course Code: ECC304 and Course Name: Network Theory

Time: 2 hour Max. Marks: 80

| Question<br>Number | Correct Option (Enter either 'A' or 'B' or 'C' or 'D') |
|--------------------|--|
| Q1.                | В  |
| Q2.                | В  |
| Q3.                | D  |
| Q4                 | С  |
| Q5                 | A  |
| Q6                 | В  |
| Q7                 | A  |
| Q8.                | C  |
| Q9.                | С  |
| Q10.               | D  |
| Q11.               | A  |
| Q12.               | С  |
| Q13.               | D  |
| Q14.               | В  |
| Q15.               | D  |
| Q16.               | С  |
| Q17.               | A  |
| Q18.               | С  |
| Q19.               | D  |
| Q20.               | A  |